

Model Name: P43T-ES3G REV:1.0

SHEET

TITLE

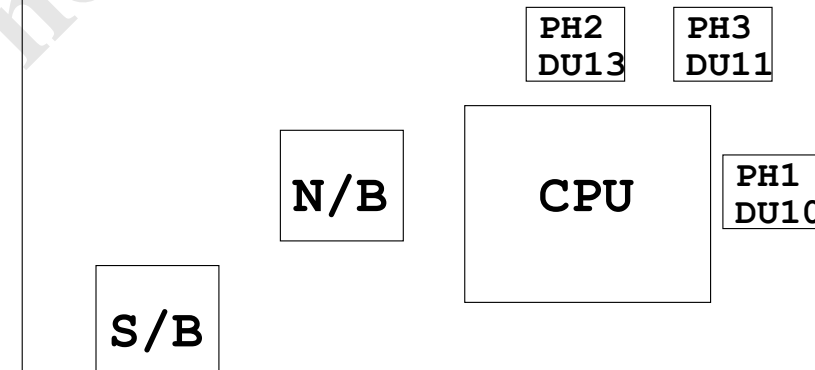
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	TABLE LIST
05	P4 LGA775 A
06	P4 LGA775 B,D
07	P4 LGA775 C
08	P4 L775 E,F,G,H
09	GMCH-Eaglelake HOST
10	GMCH-Eaglelake DDRIII
11	GMCH-Eaglelake PCI E, DMI
12	GMCH-Eaglelake INT VGA
13	GMCH-Eaglelake GND
14	GMCH-Eaglelake PWR
15	DDRIII CHANNEL A 1,2
16	DDRIII CHANNEL B 1,2
17	DDRIII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH10 DMI, PCI, USB
20	ICH10 GPIO, CTRL
21	ICH10 SATA, FAN PWM
22	ICH10 VCC, GND
23	CLOCK-REALTEK 587
24	PCI SLOT 1, 2, PCIEX1 1
25	ITE8718/GB,RESET DRIVE
26	COM LPT, -PROHOT,DYNAMIC,RUSB
27	BIOS,CI,HWM,KB/MS

SHEET

TITLE

28	AZALIA ALC888
29	AUDIO JACK
30	VCORE PWM ISL6334CRZ
31	DISCRETE1 POWER,FAN CTRL
32	ATX POWER
33	JMicron JMB368
34	LAN REALTEK RTL8111D
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2
37	PCI SLOT 3, 4 , 5

PWM各相位的擺法如下:



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Cover Sheet			
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Model Name: GA-P43T-ES3G

Rev:.1.0

Component value change history

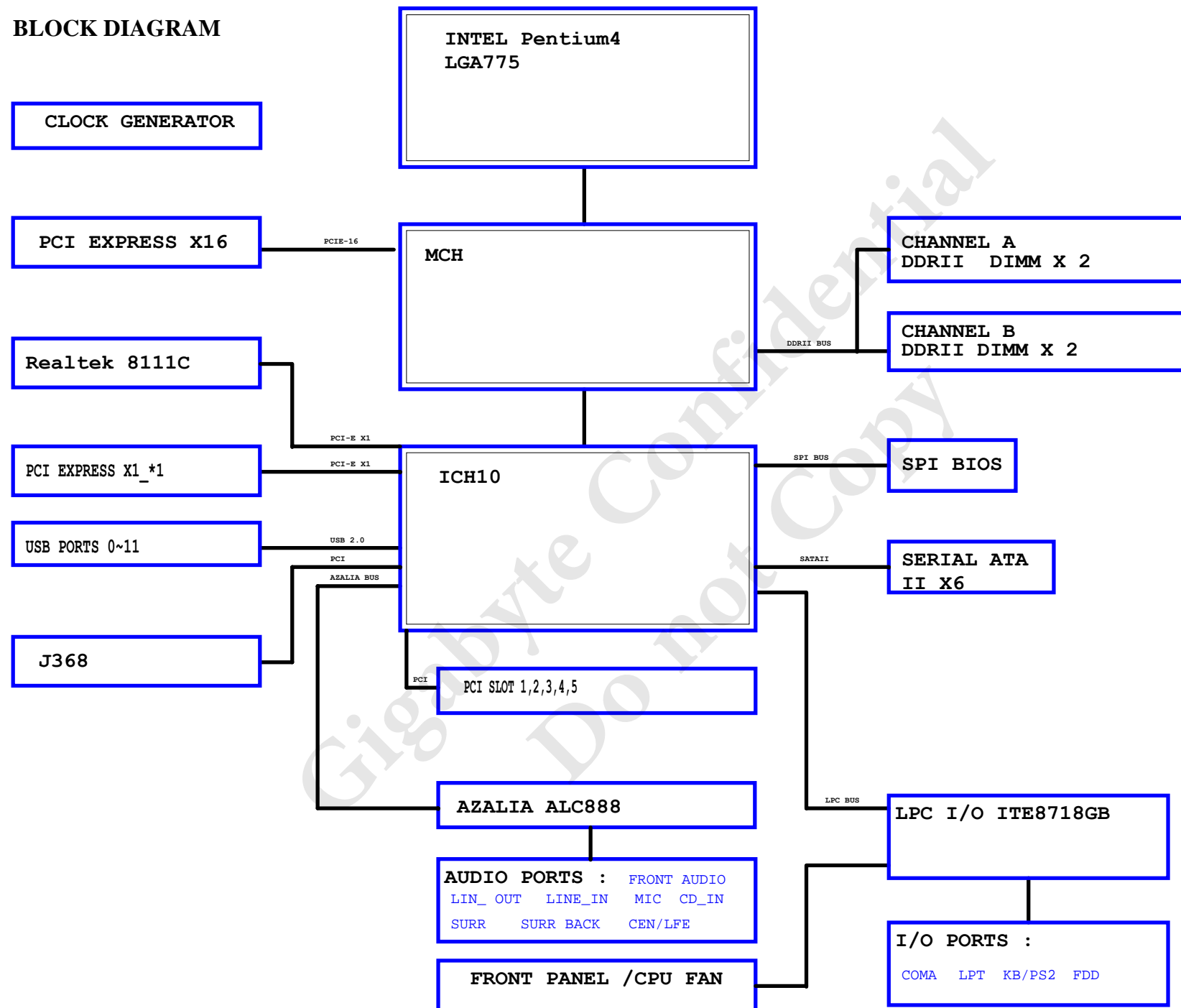
Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的OWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V>2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
	3. CE2,CE3 EC-CAP---->FP-CON CAP FOR CPU FAN ISSUE	
97/05/13 PBOM:10C	1. ADD BACKUP BIOS AND RESISTOR	
97/05/21 PBOM:10D	1. ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/04 PBOM:10E	1.Q49 BAT54C限用DII FOR STR ISSUE	
97/06/18 PBOM:10F	1.C197 0.1U/Y5V--->0.1U/X7R	
	2.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/07/22 PBOM:10G	1.換NEW P43 A2 CHIP	
97/08/11 PBOM:10H	1.由10E 改; RR2 68--->44.2 FOR J368 1.8V	
97/09/24 EBOM:01	1.E-BOM FOR P43-ES3G-0.1	
97/10/24 EBOM:10A	1.LBC34 100PF----->0 ohm for EMI issue	
	2.DEL R132,R133,Q1,Q2,R58,R59 FOR non CIA2 function	
97/11/07 PBOM:10B	1.FDD 改爲白色 2.改BC38,BC65 改爲1UF	
98/04/24 PBOM:10D	1.部份阻值改爲1%,	
98/05/07 PBOM:10E	1.D8 改成OLD BAT54A,R282 PULL LOW,R323,R330移除	
98/05/25 PBOM:10F	1.D7,D9,D11,D4,D6,D13改成OLD BAT54A	
	1.ADD EUP FUNCTION	
	2.CODEC CO-LAY,ADD EOS protect diode	
	3.8111C---->8111D	
P43T-ES3G-10A	1. PCB內容有誤,包材修改	

Circuit or PCB layout change
for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/08/08 PCB:1.01	1.DDR1200 OC 文字面改爲DDR 1200	
97/09/23 PCB:0.1	1.由EP43-DS3L-1.01修改成GA-P43-ES3G-0.1	
	2.CPU VCORE 改爲3相	
	3.後窗改爲 1 serial port ,parallel port,aduio 爲 analog 3 port,digital 只有同軸,USB *6, 前窗USB *6	
	4.support easy saver function;PCI SLOT*5	
97/10/30 PCB:1.0	1.GA-P43-ES3G-1.0 FOR PVT	
98/04/15 PCB:1.01	1.GA-P43-ES3G-1.01 修改LL1電感位置	
2009/10/06 PCB:1.1	1.ADD EUP FUNCTION	
	2.CODEC CO-LAY,ADD EOS protect diode	
P43T-ES3G-10A	1. F_PANEL是否要改新的	

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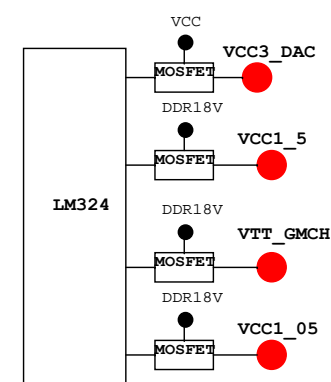
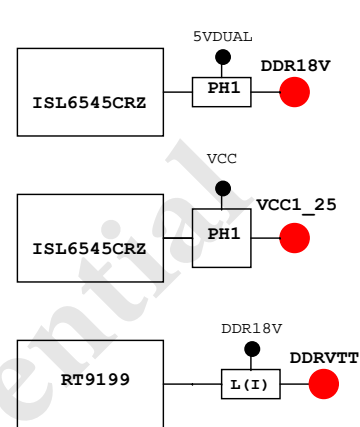
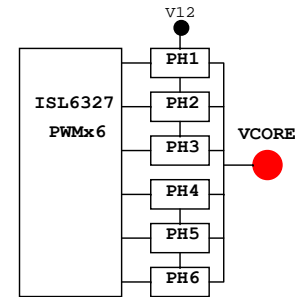
Title BOM & PCB MODIFY HISTORY		
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BLOCK DIAGRAM

ICH8 GPIO LIST TABLE

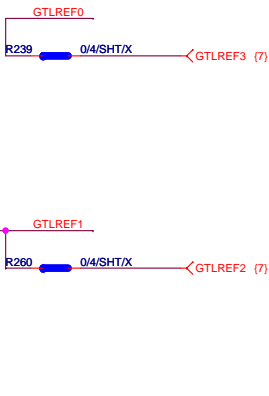
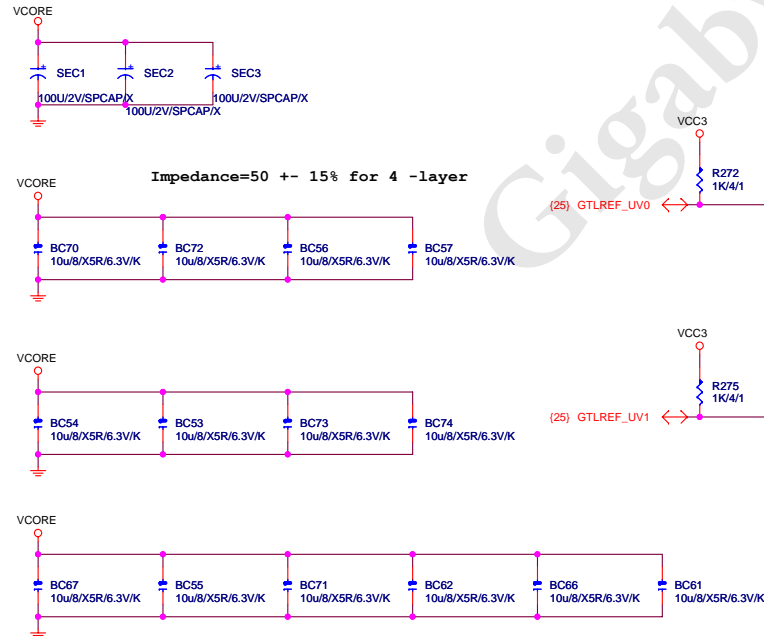
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8 (DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE (STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2 (STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27 (EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED (EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:6 PHASE PWM--ISL6327CRZ

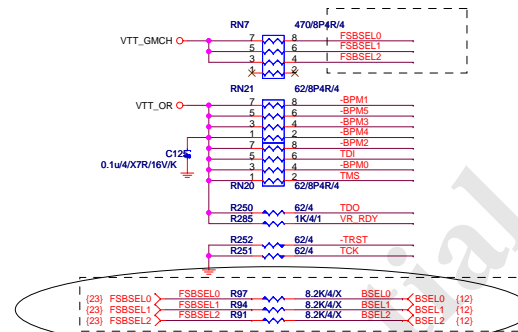


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Title		TABLE LIST	
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SP-CAP X 3PCS

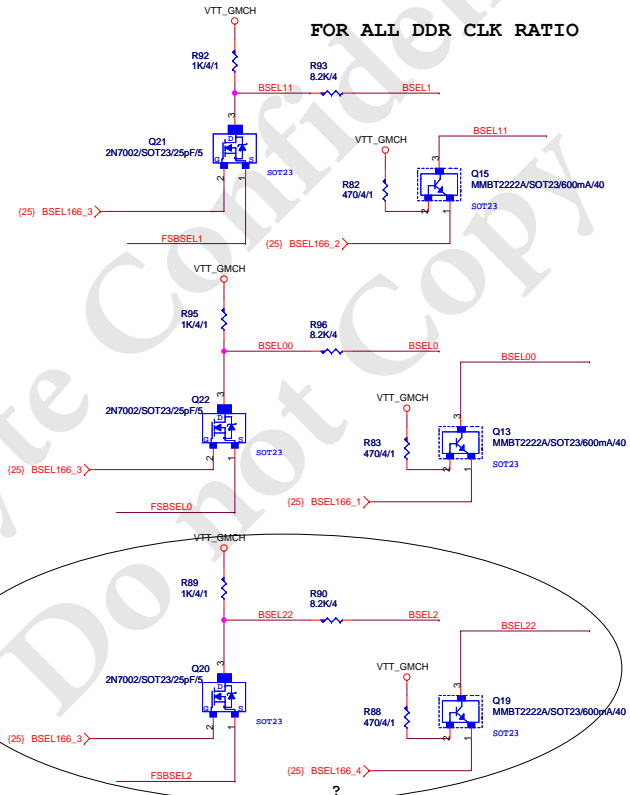


CPU GTLREF RATIO		
GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615



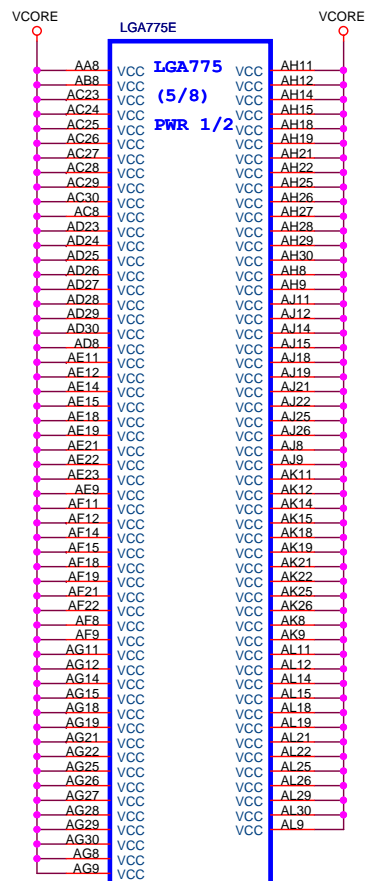
FORCE 400MHz CPU TO 333MHz

FOR ALL DDR CLK RATIO

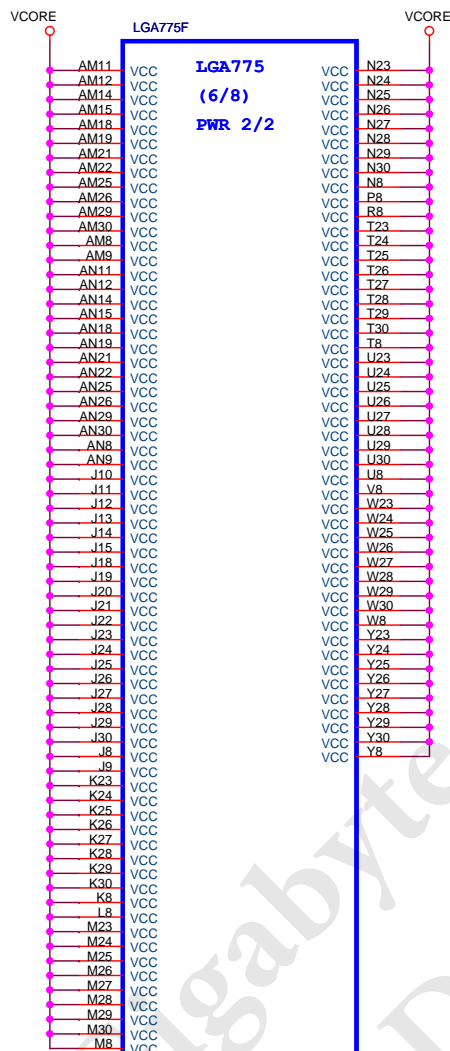


	FSA	FSB	FSC		
	FSBSEL0	FSBSEL1	FSBSEL2	Clock	
?	1	0	1	100MHz	
?	1	0	0	133MHz	3/4
G33	0	1	0	200MHz	2/2.66/3.33/4#
G33	0	0	0	266MHz	2/2.5/3/4~
G33	0	0	1	333MHz	2/2.4/3.2/4#
	0	1	1	400MHz	

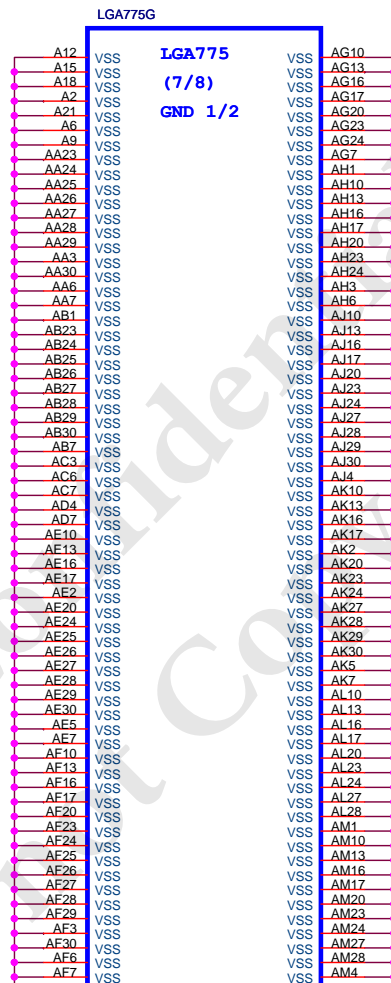
PECI:Platform Environment Control Interface



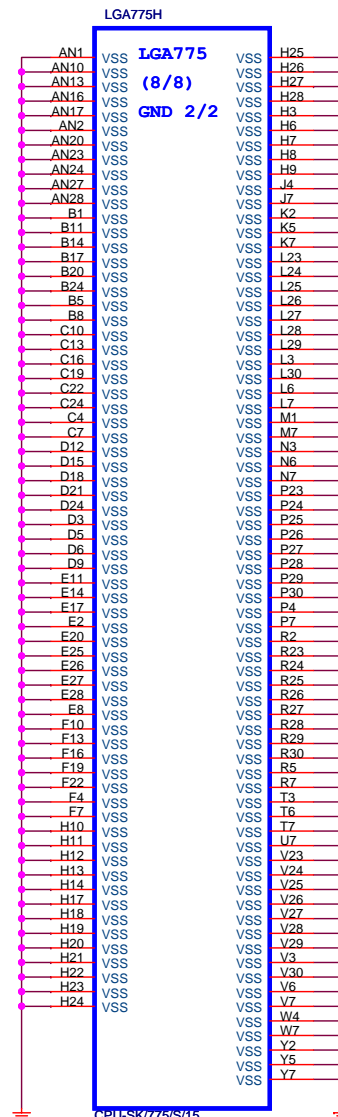
CPU-SK/775/S/15



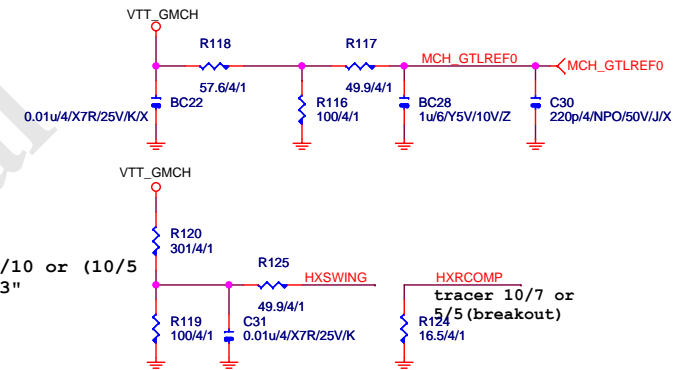
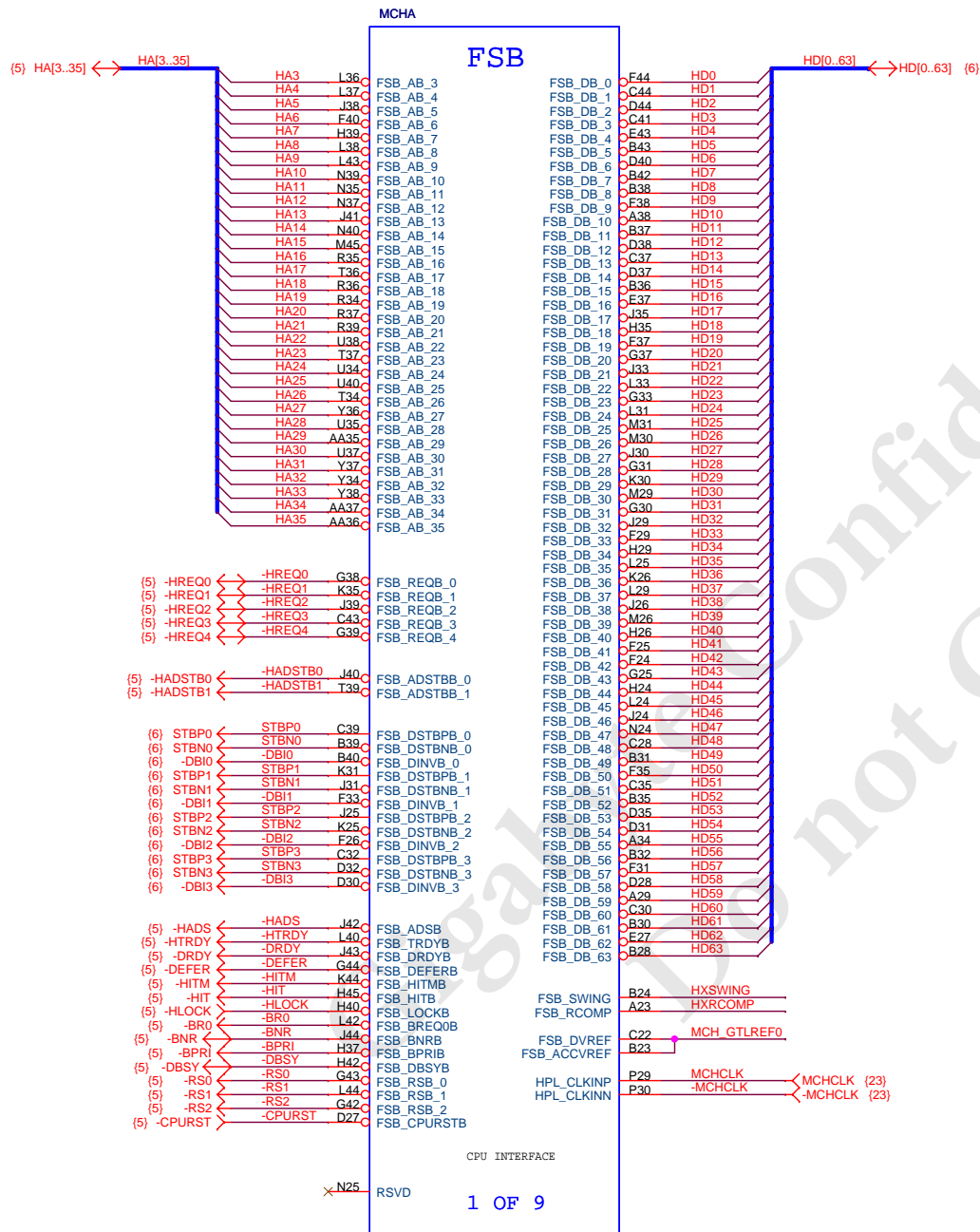
CPU-SK/775/S/15



CPU-SK/775/S/15



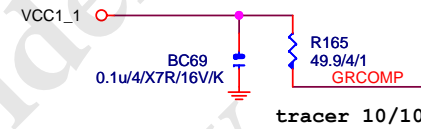
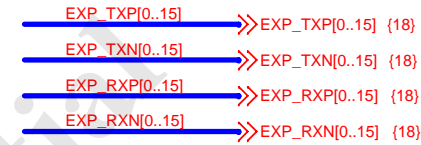
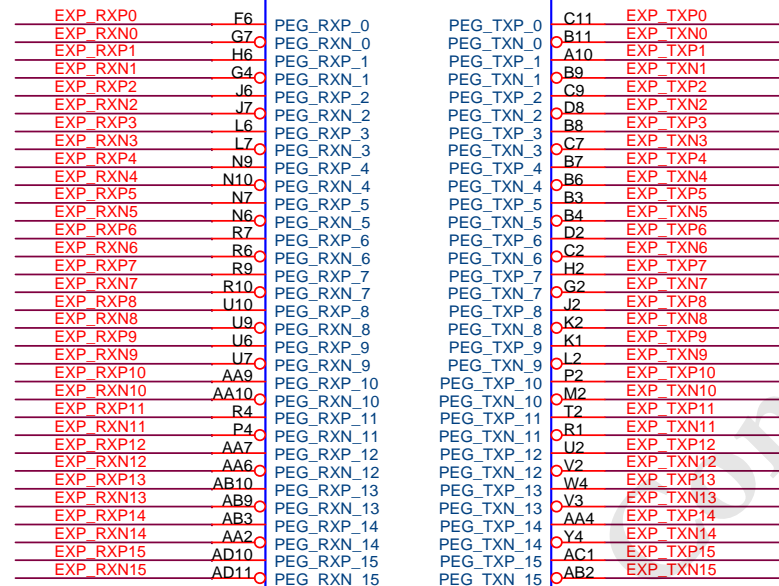
CPU-SK/775/S/15





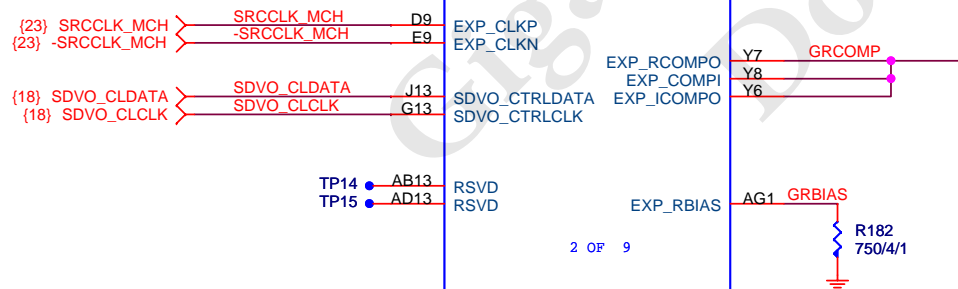
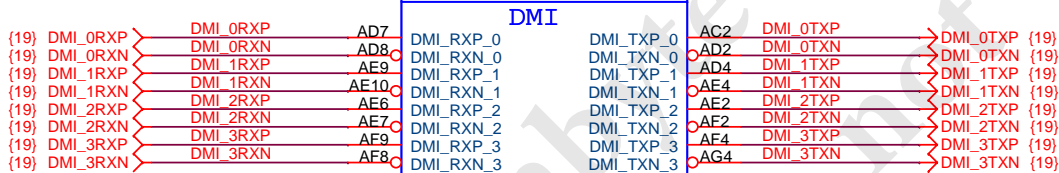
PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)

Impedance=85 +- 17.5%



DMI:12/4/8/4/12

Impedance=95 +- 17.5%



AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

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GMCH-PCI E & DMI		
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EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE

EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

ITPM:

0:ENABLE ITPM
1:DISABLE ITPM

CEN:

0:DISABLE TLS
1:ENABLE TLS

MCHE

VGA

MISC

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AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

CRT_HSYNC
CRT_VSYNC

CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTN

CRT_DDC_DATA
CRT_DDC_CLK

DAC_IREF

DPL_REFCLKINP
DPL_REFCLKINN
DPL_REFSSCLKINP
DPL_REFSSCLKINN

RSVD
RSVD
NC
RSTINB
PWROK
ICH_SYNCB

HDA_BCLK
HDA_RSTB
HDA_SDI
HDA_SDO
HDA_SYNC

DDPC_CTRLCLK
DDPC_CTRLDATA

DPRSTPB
SLPB

D14
C14

B18
D18
C18
F13

L15
R110
M15
R109

B15

E15
D15
G8
G9

L13
L11
B14
AN6
AR4
K15

AU4
AV4
AU2
AV1
AU3

J11
F11

P43
P42

B45
AK15
AD42
AN16
W30
AW44
R42
U32

VCC3

VCC1_1

R127
R126

-PFMRST1
PWROK1

0/8P4R/0402/SHT/X

0/4/SHT/X

VCC3

R108
1K/4/X

C28
1n/4/X7R/50V/K/X

BW+ICH8
BW+ICH7

-PFMRST1

C91
22p/4/NPO/50V/J/X

PWROK1

C92
22p/4/NPO/50V/J/X

-ICHSYNC

C87
1n/4/X7R/50V/K

Gigabyte Technology

Title

GMCH-INTERNAL VGA

Size
Custom

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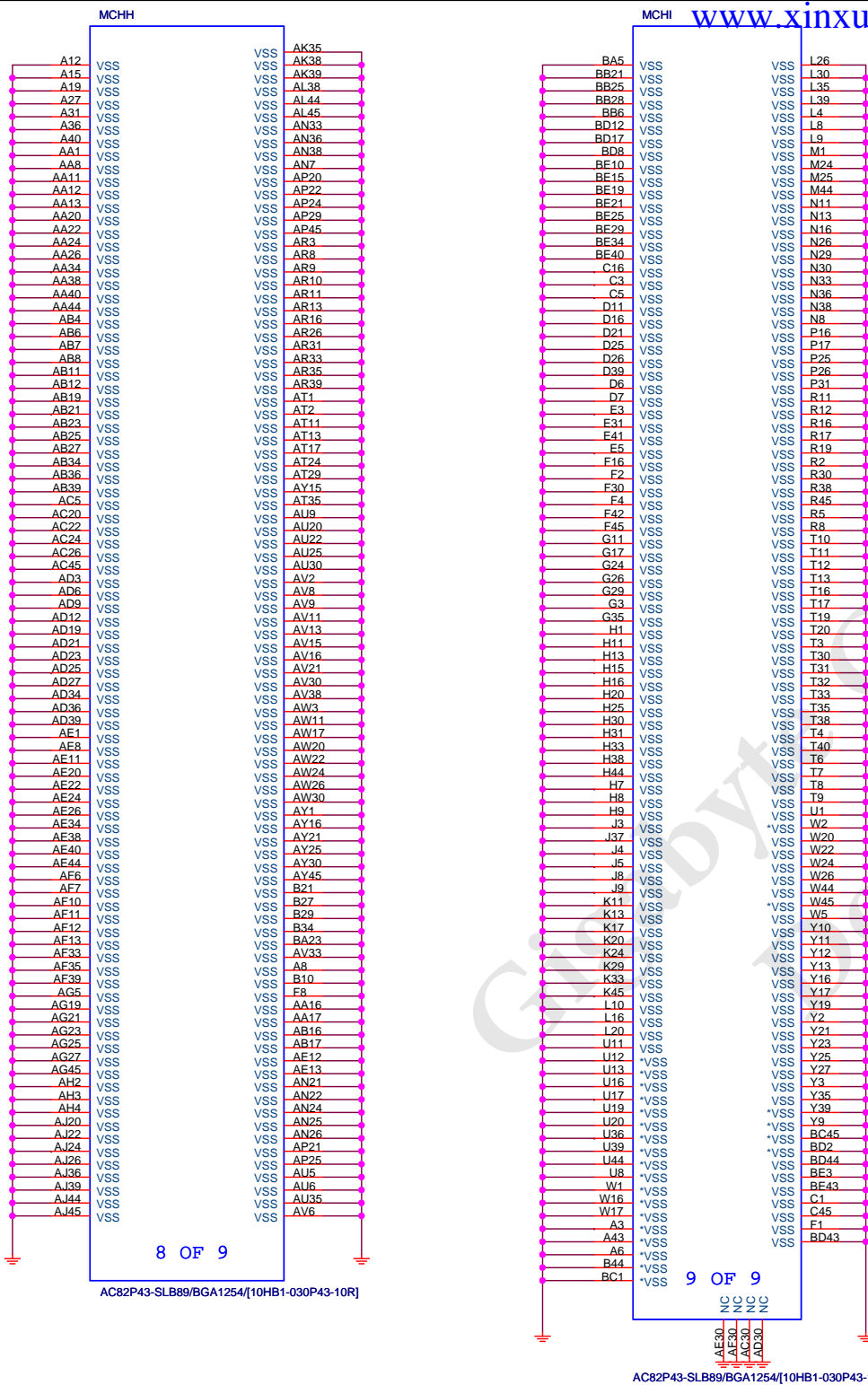
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GMCH-GND

Size

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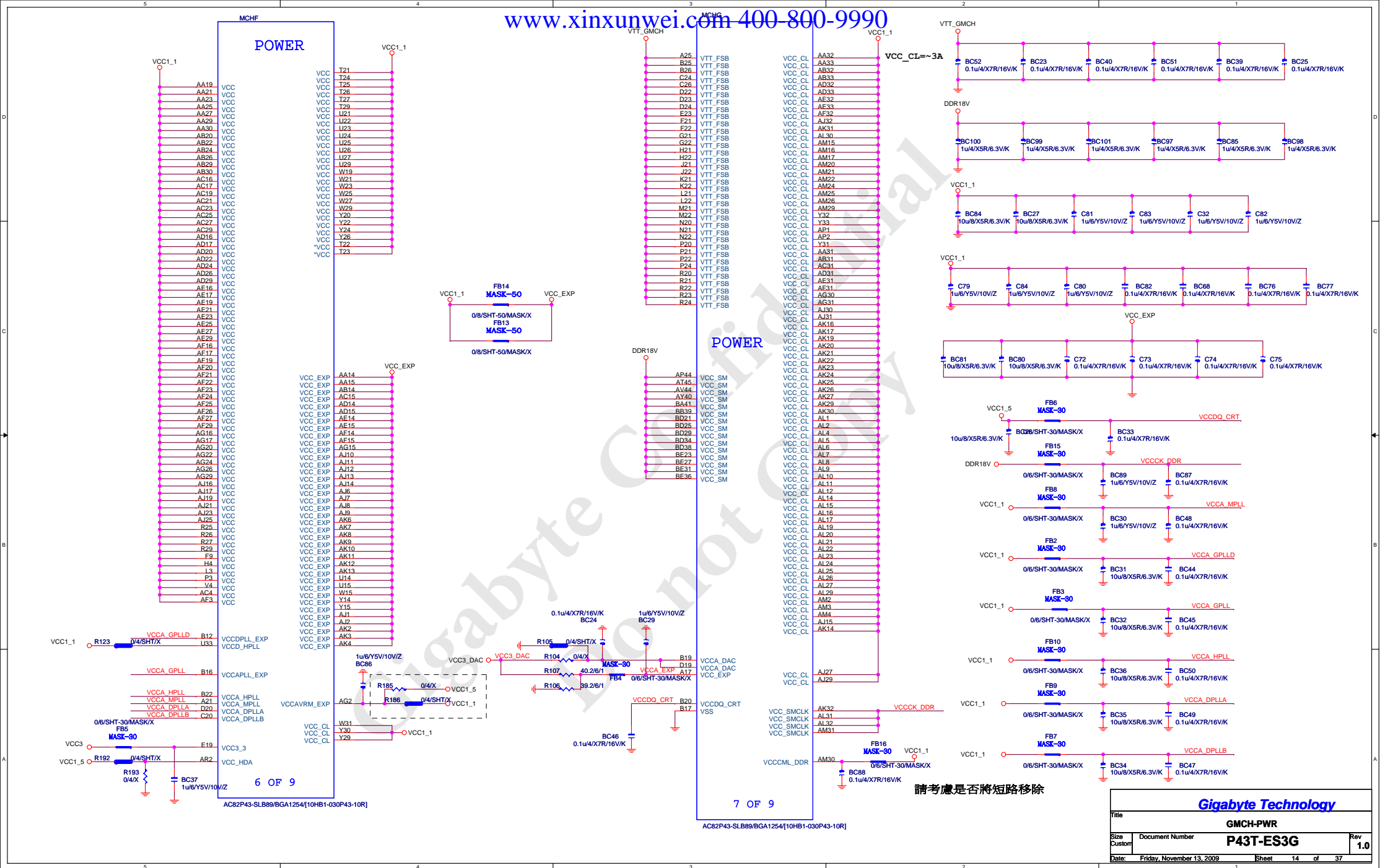
13

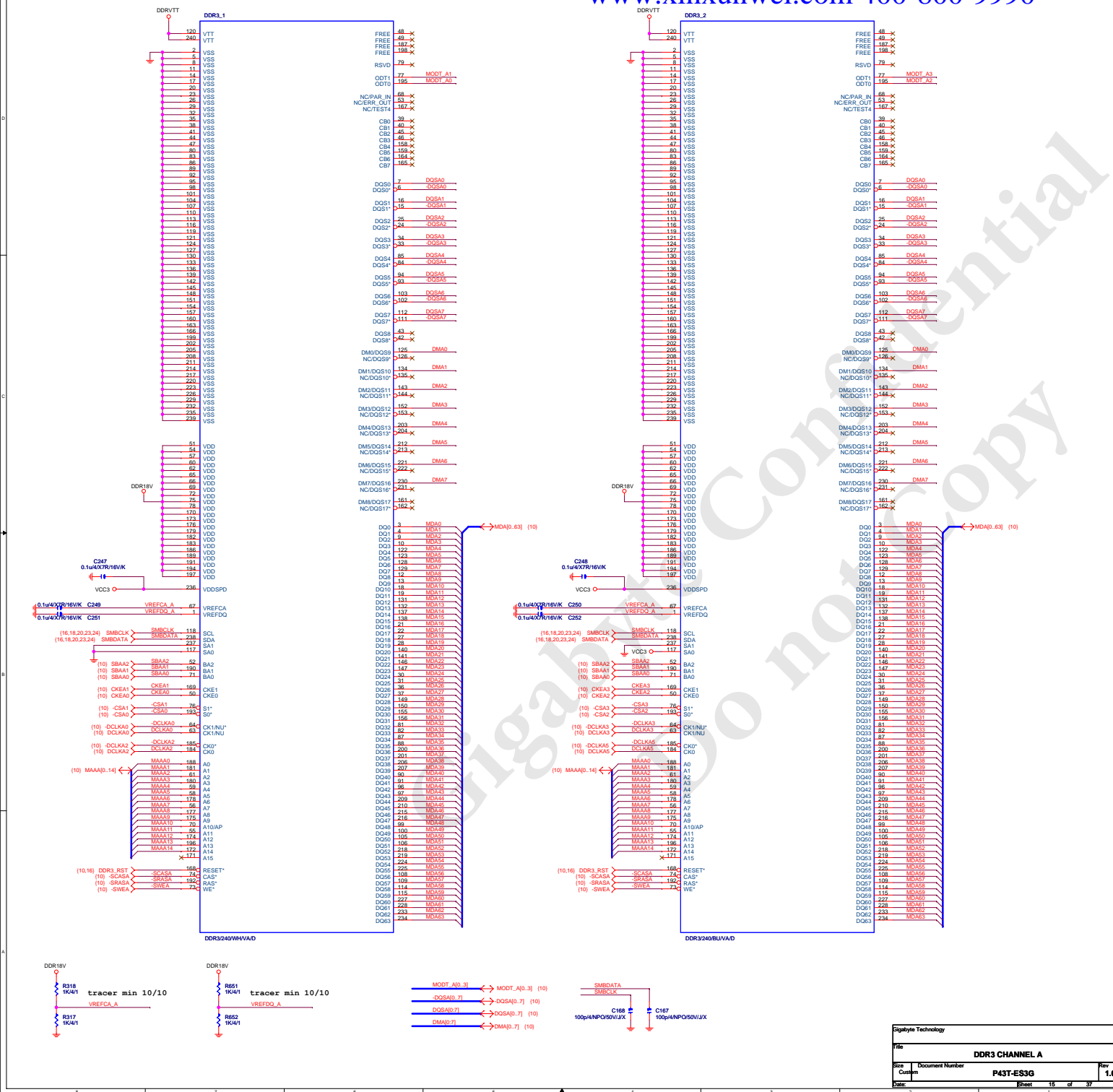
of

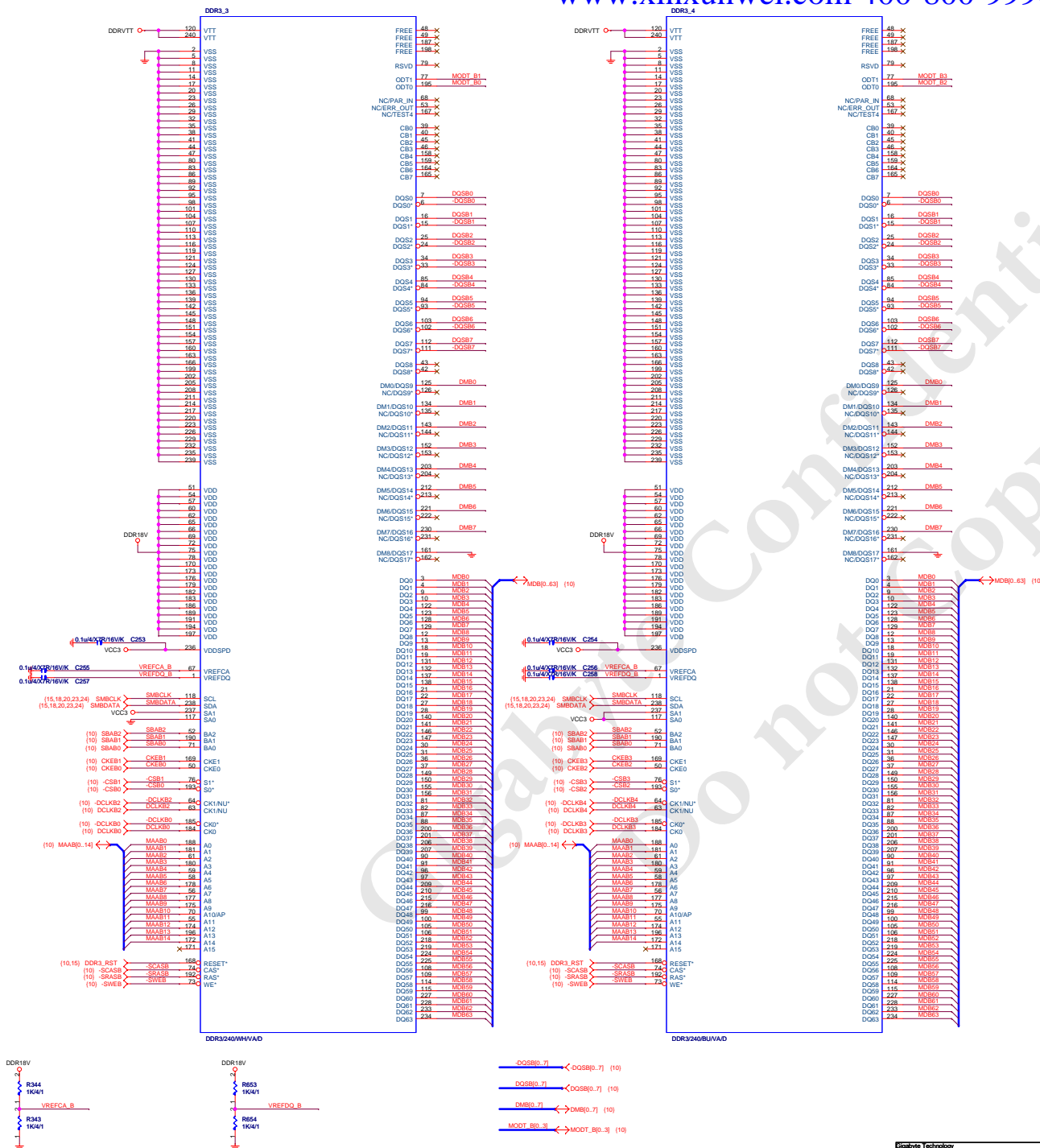
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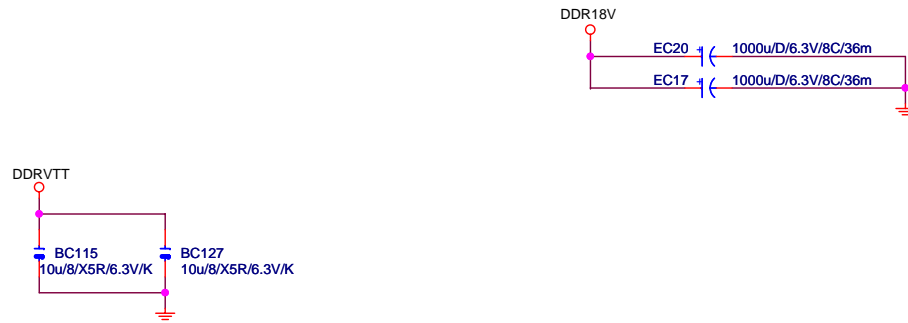




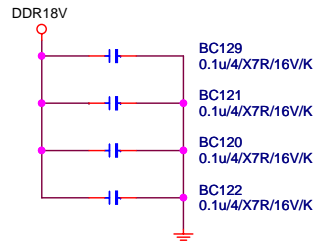


DDR TERMINATION CHANNEL A

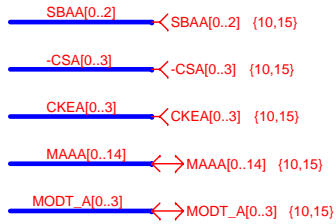
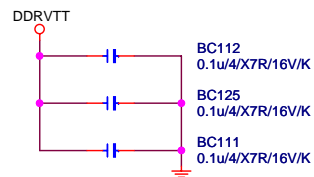
DDRVTT Decouple



DDR18V Decouple

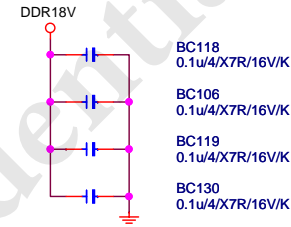


DDRVTT Decouple

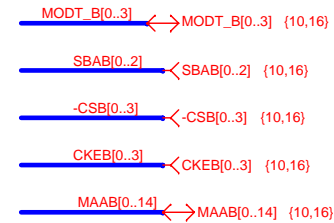
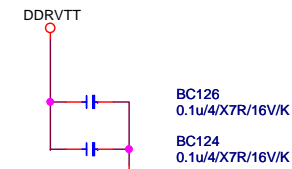


DDR TERMINATION CHANNEL B

DDR18V Decouple



DDRVTT Decouple



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Title

DDR3 TERMINATOR

Size
Custom

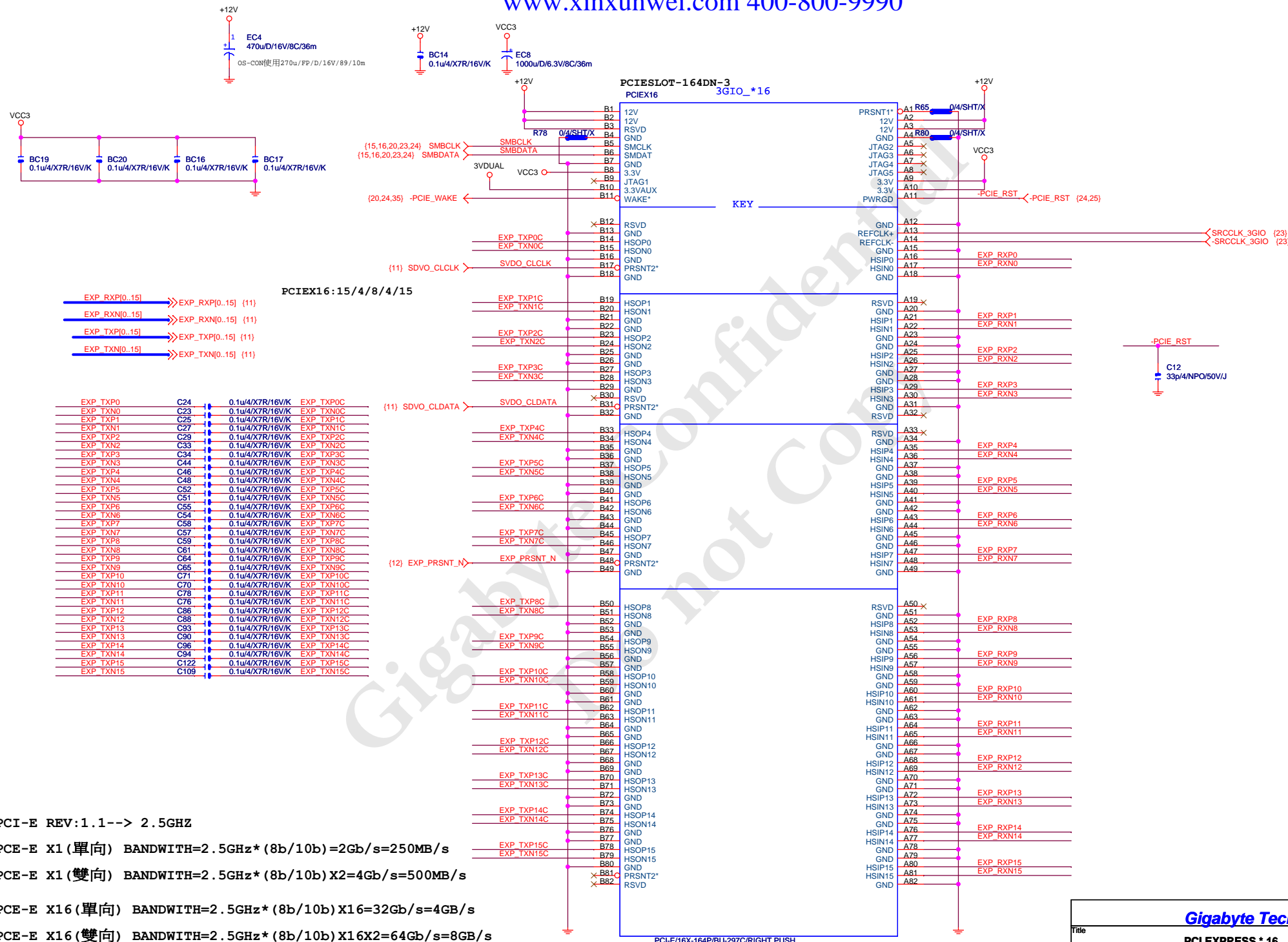
Document Number

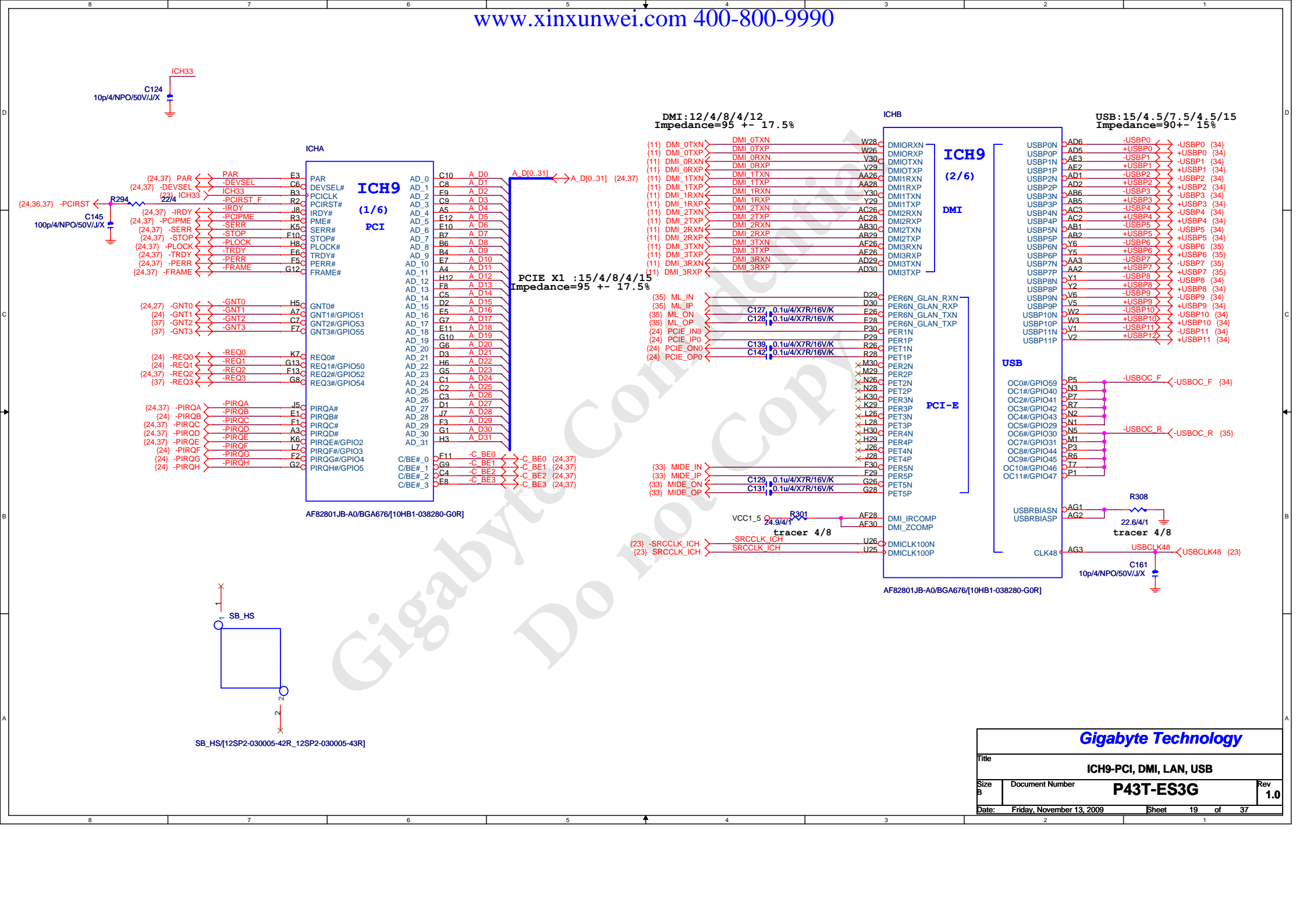
P43T-ES3G

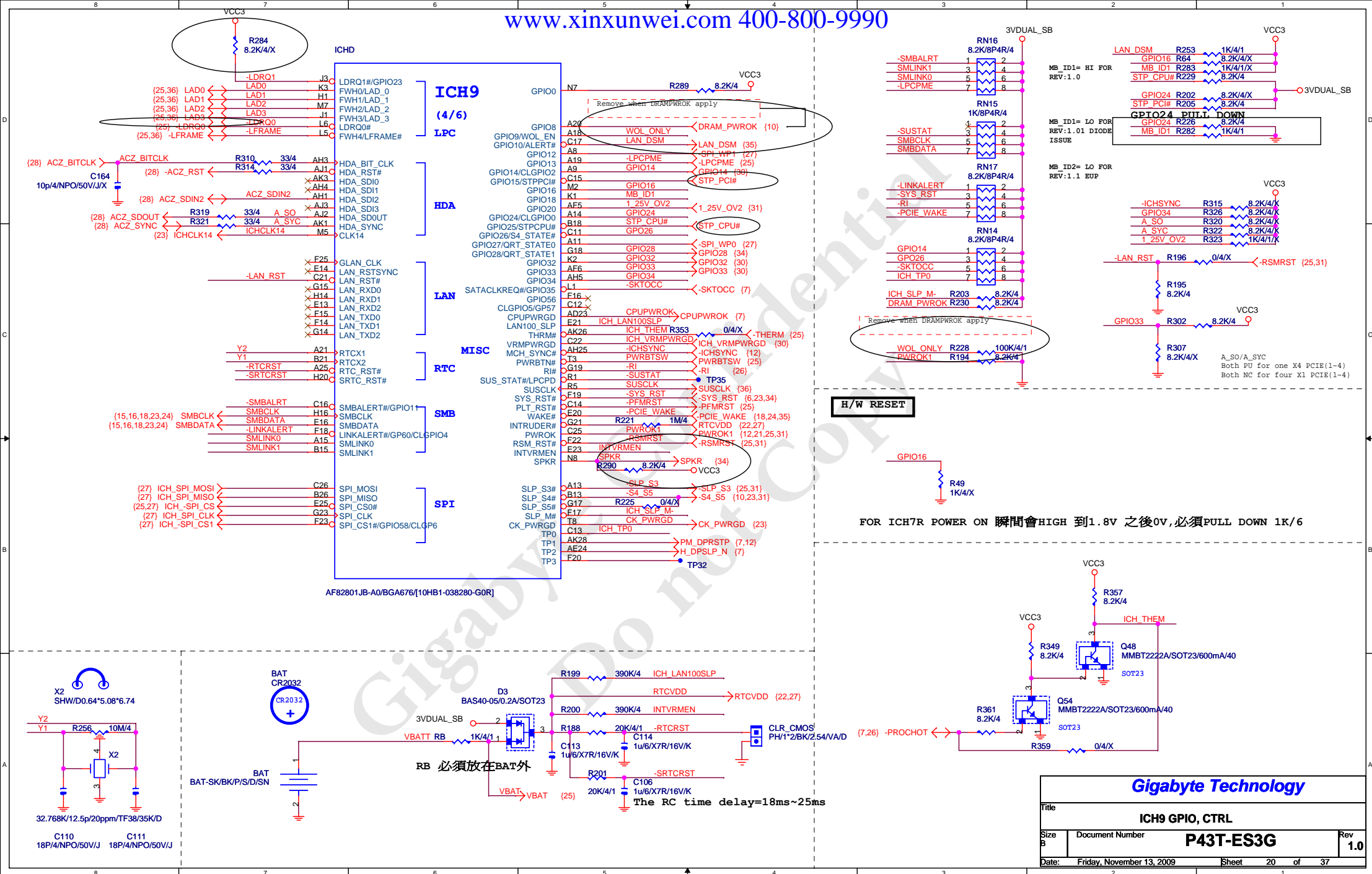
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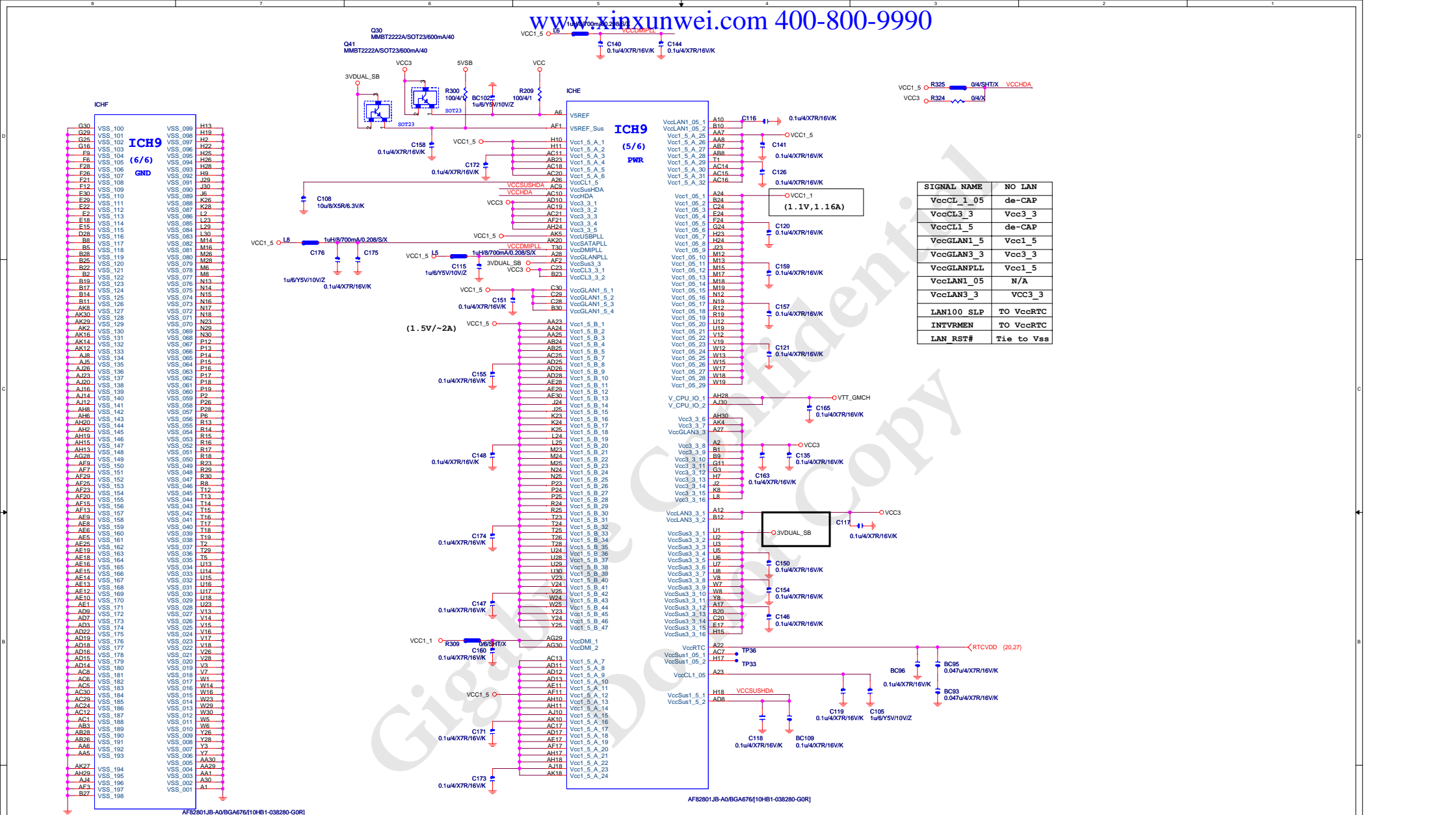
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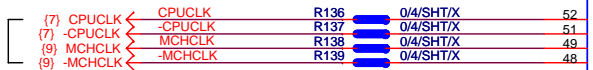


CL_VREF:4/10
0.405V

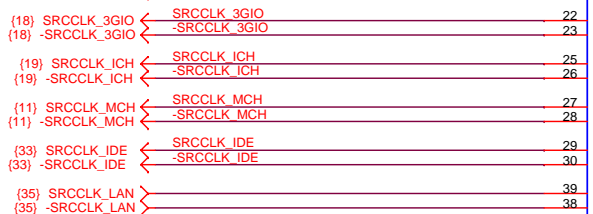


CLK GEN CK505

50歐姆: [18/4/10/4/18]



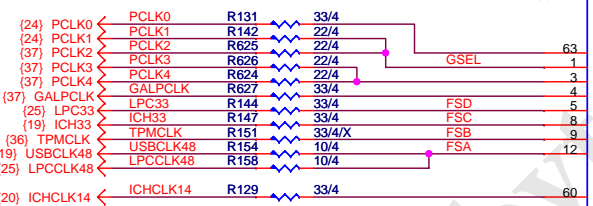
50歐姆: [18/4/10/4/18]



50歐姆: [18/4/10/4/18]

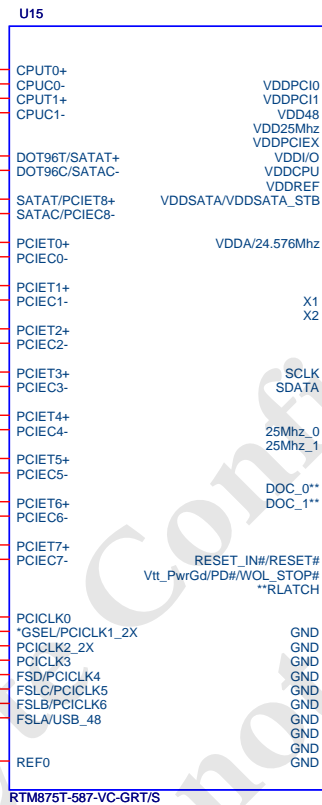


50歐姆: [4/10]

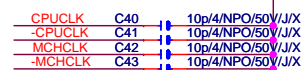
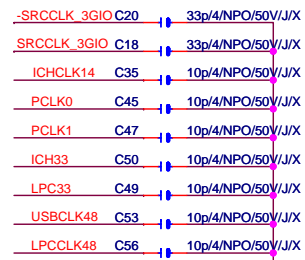
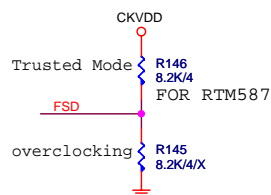
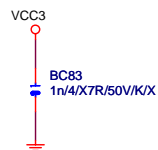
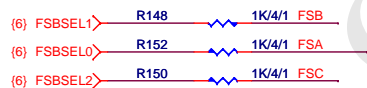


50歐姆: [4/10]

50歐姆: [4/10]



GSEL=1,96Mhz from 14/15,SATACLK from 17/18
 GSEL=0,SATACLK from 14/15,PCIECLK from 17/18



GSEL=1,96Mhz from 14/15,SATACLK from 17/18
 GSEL=0,SATACLK from 14/15,PCIECLK from 17/18

Gigabyte Technology

CK505 CLK GEN

P43T-ES3G

Title

Size
Custom

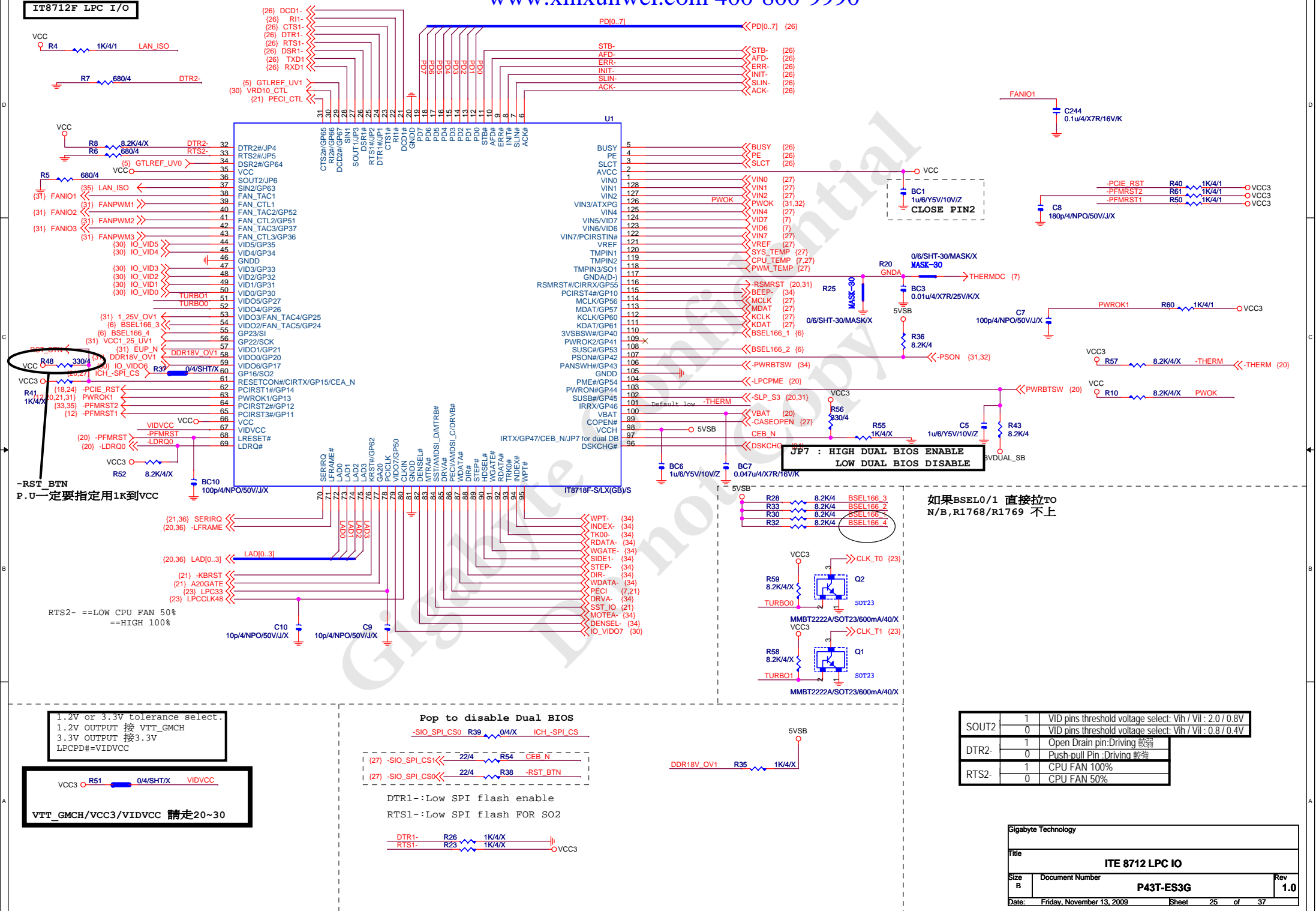
Document Number

Rev
1.0

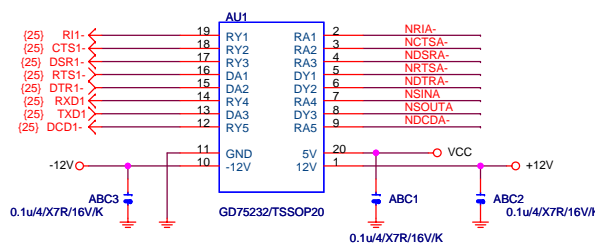
Date: Monday, November 16, 2009

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IT8712F LPC I/O

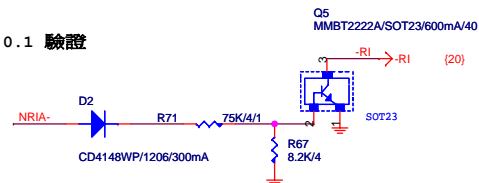


COMA

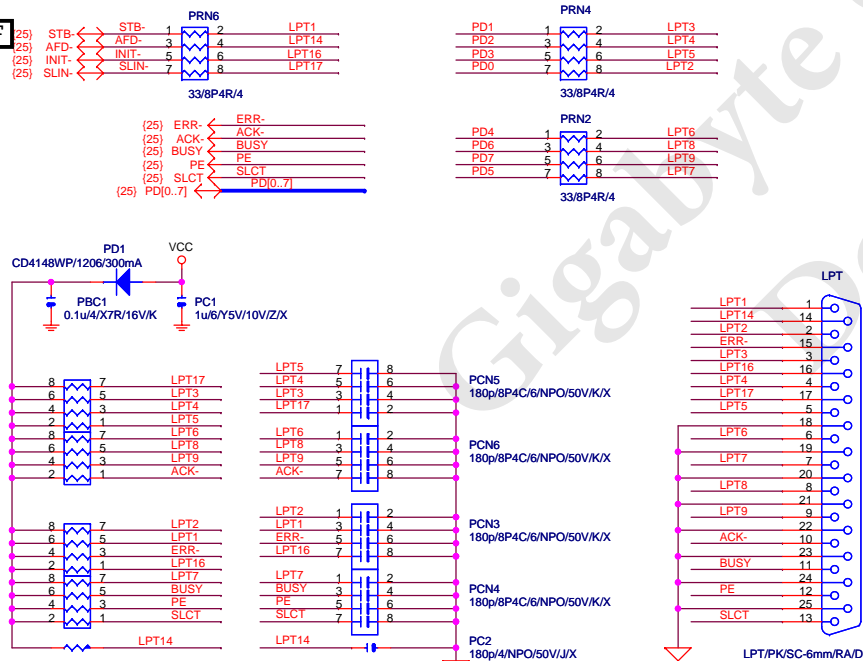


COM RT

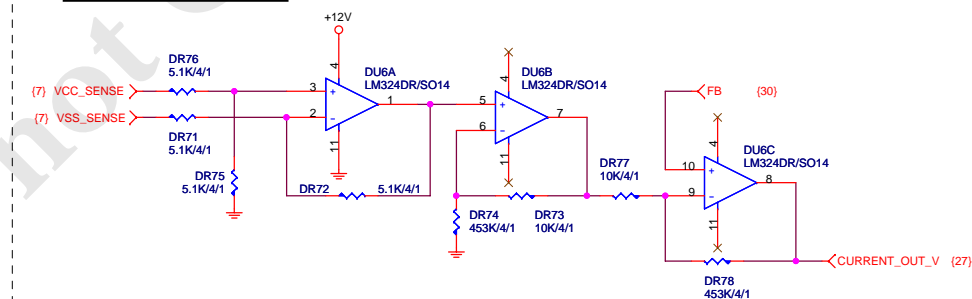
REV:0.1 驗證



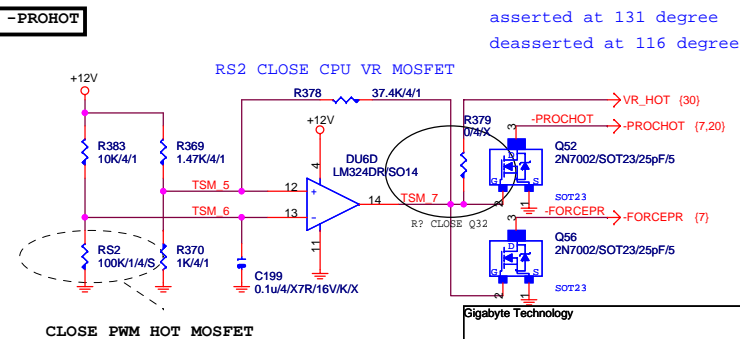
LPT PORT



DYNAMIC CURRENT OC



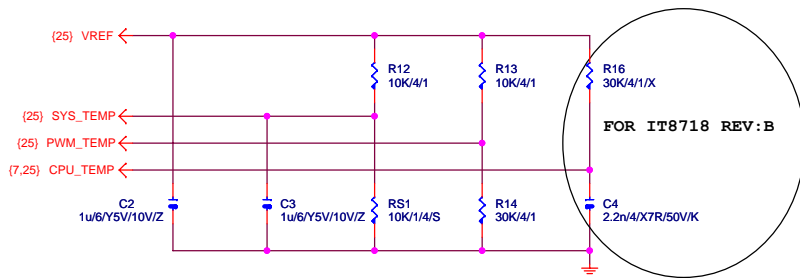
-PROHOT



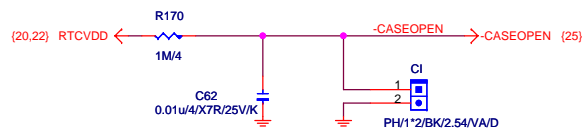
Gigabyte Technology

COM & LPT PORT			
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TEMP H/W MONITOR

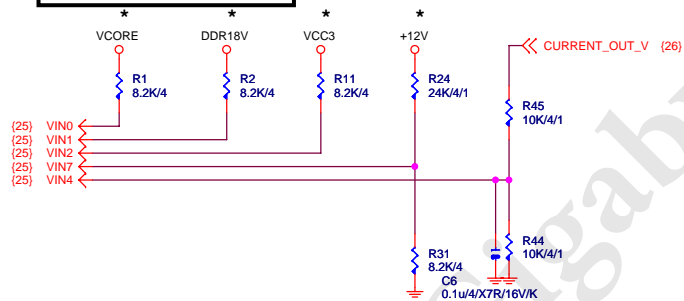


CASE OPEN

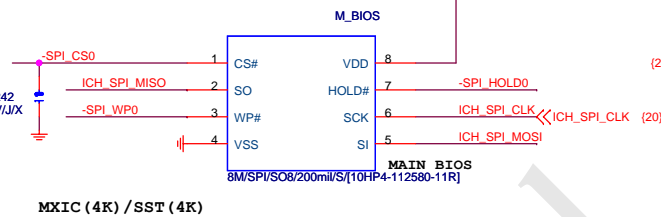
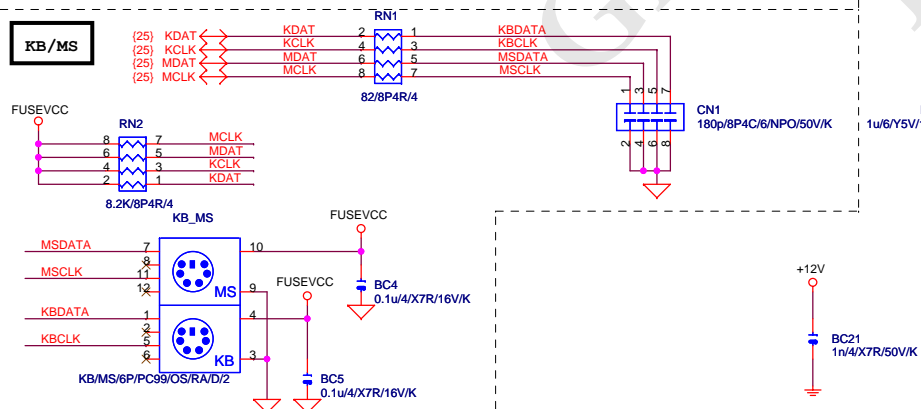


Case Open Circuits

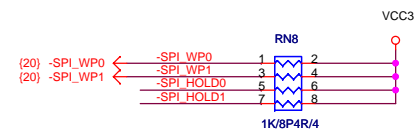
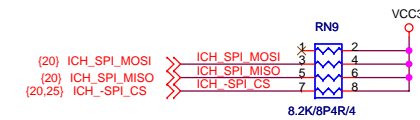
VOLTAGE-- H/W MONITOR



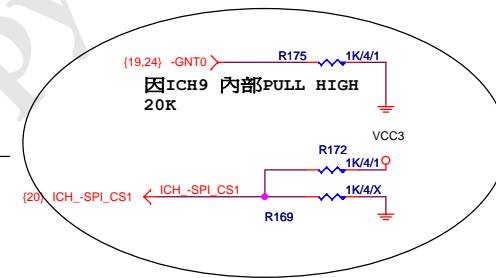
KB/MS



MXIC (4K) / SST (4K)



BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
FWH	1	1



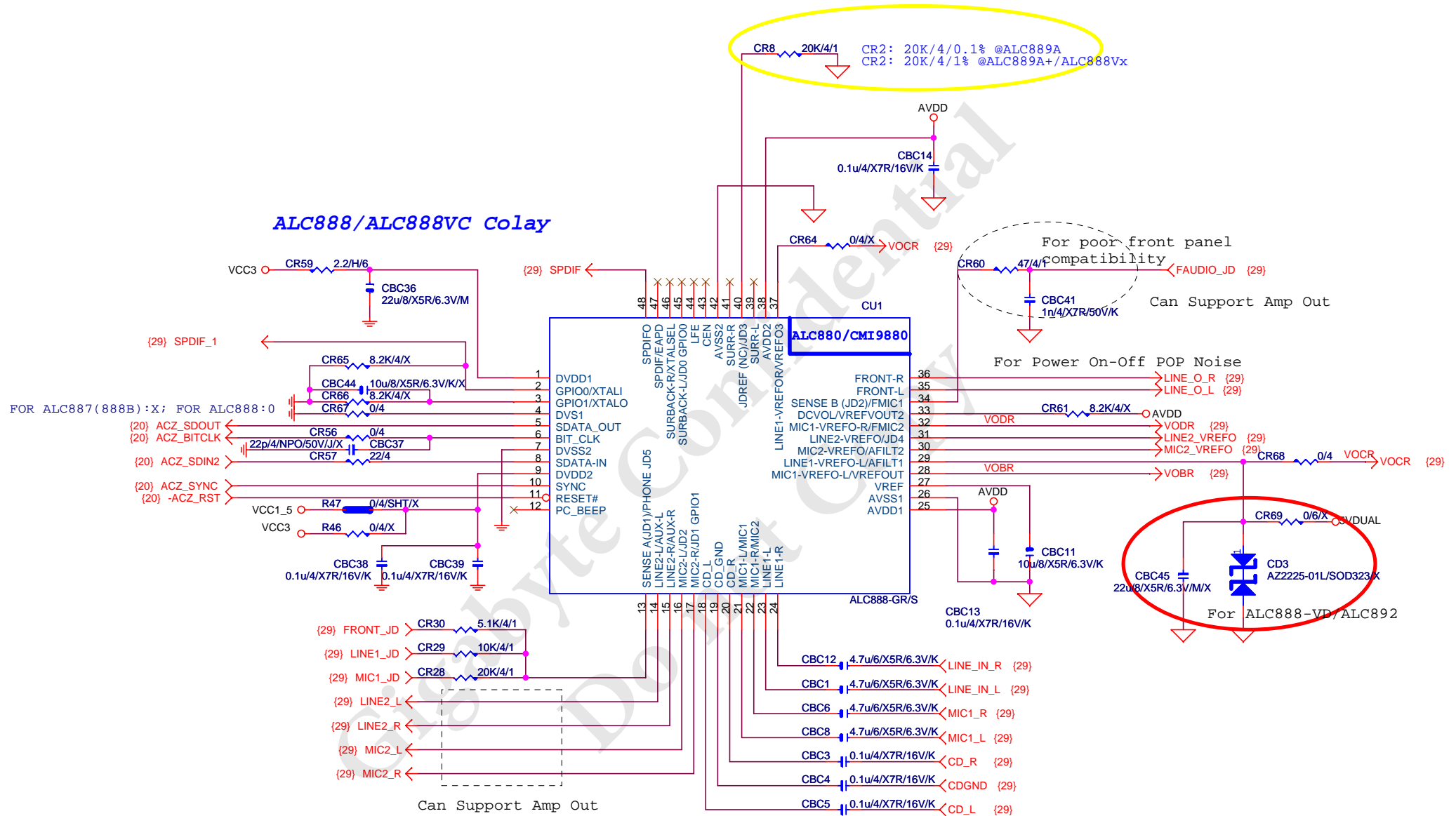
PCI_BT1



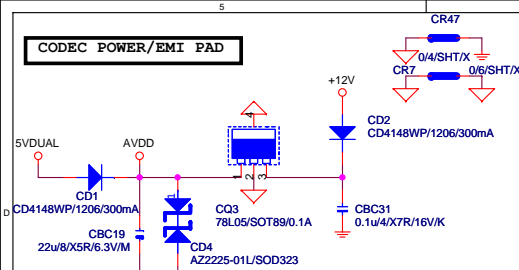
JP/1*2/BU/OH/O:[1-2]CLOSE/X

Gigabyte Technology

Title	BIOS/HW-MONITOR/CI/KB/MS		
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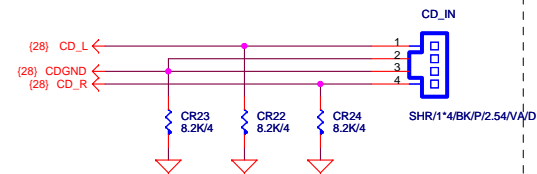


CODEC POWER/EMI PAD

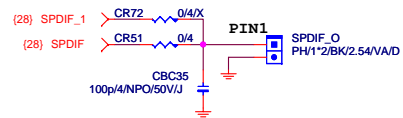


CO-LAYOUT

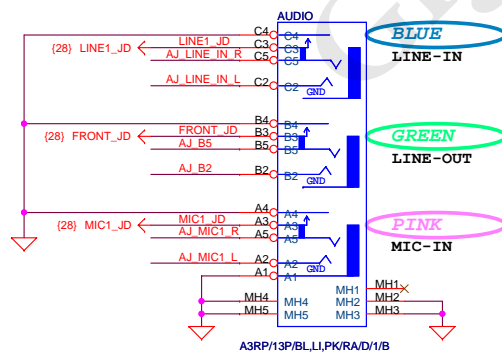
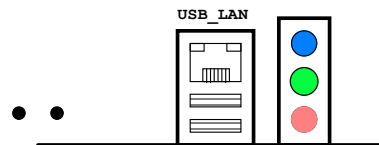
CD IN



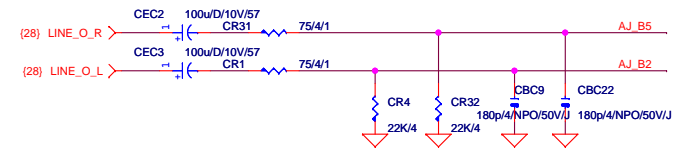
SPDIF



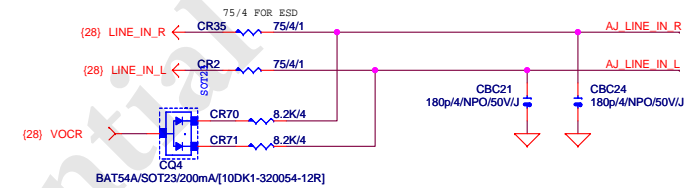
AZALIA JACK



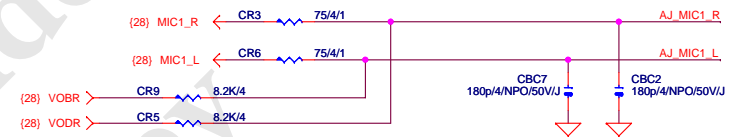
LINE-OUT



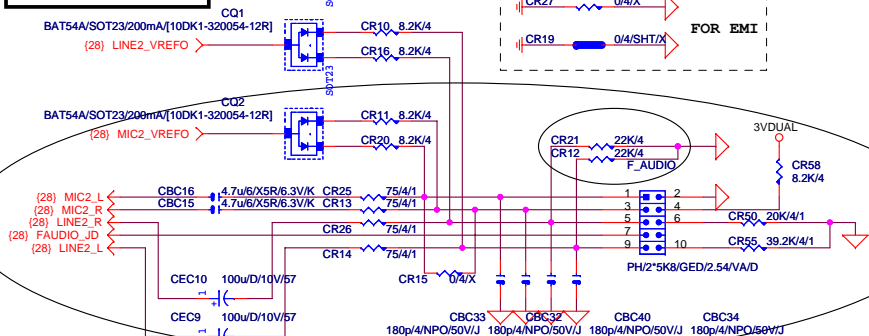
LINE-IN



MIC-IN

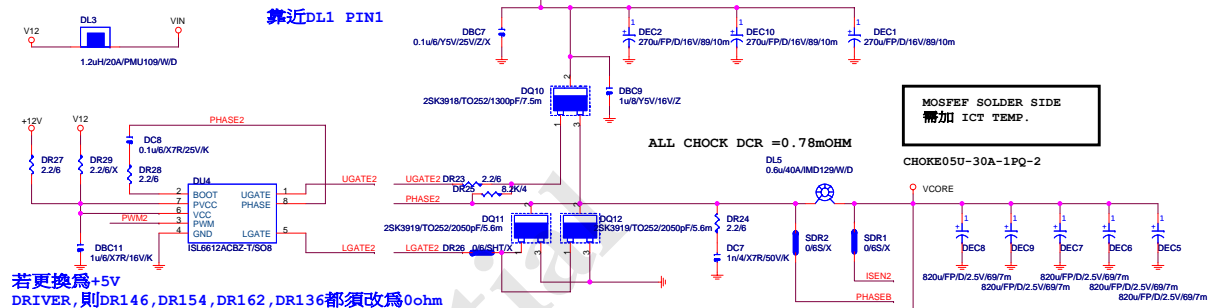


AZALIA FRONT PANEL

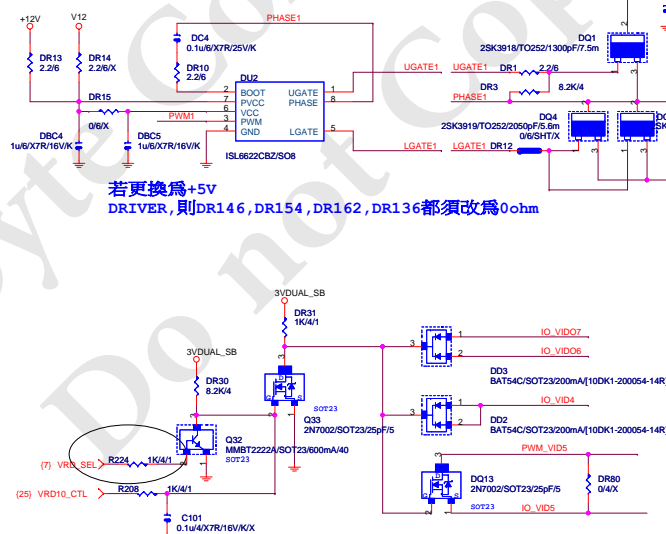
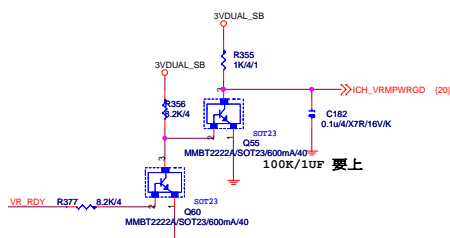


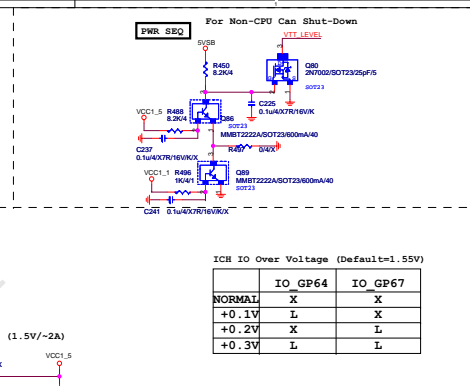
Gigabyte Technology

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AUDIO JACK		
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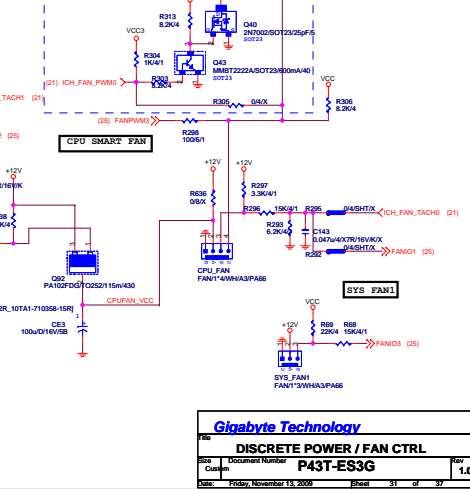
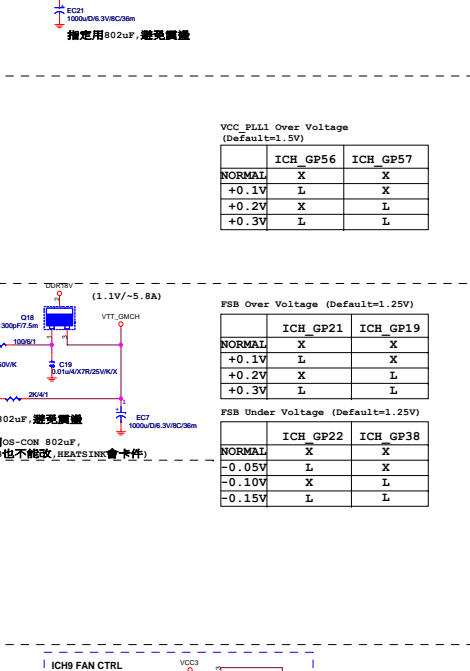
若更換為+5V DRIVER,則DR146,DR154,DR162,DR136都須改為0ohm



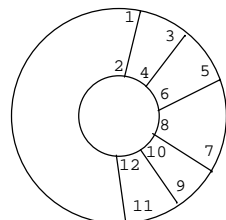
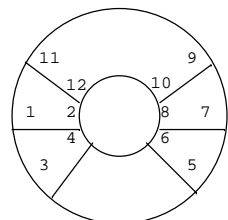
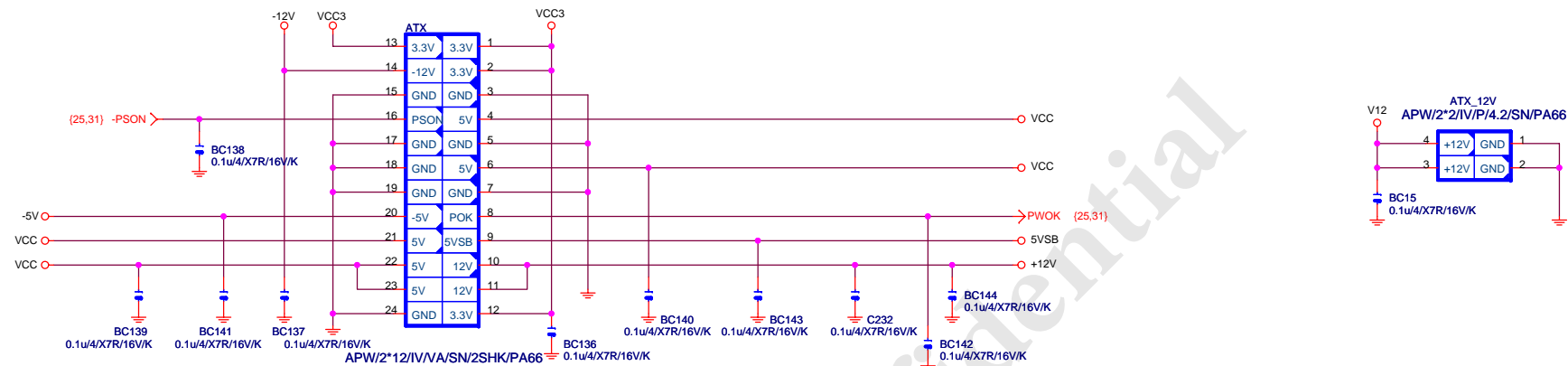


	ICH_GP56	ICH_GP57
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

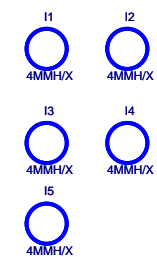
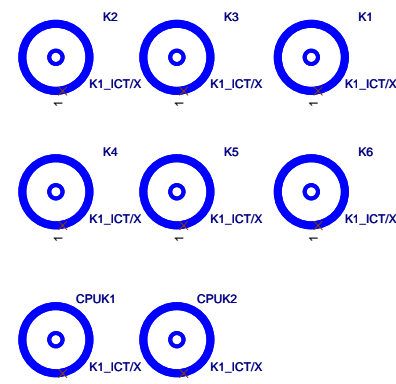
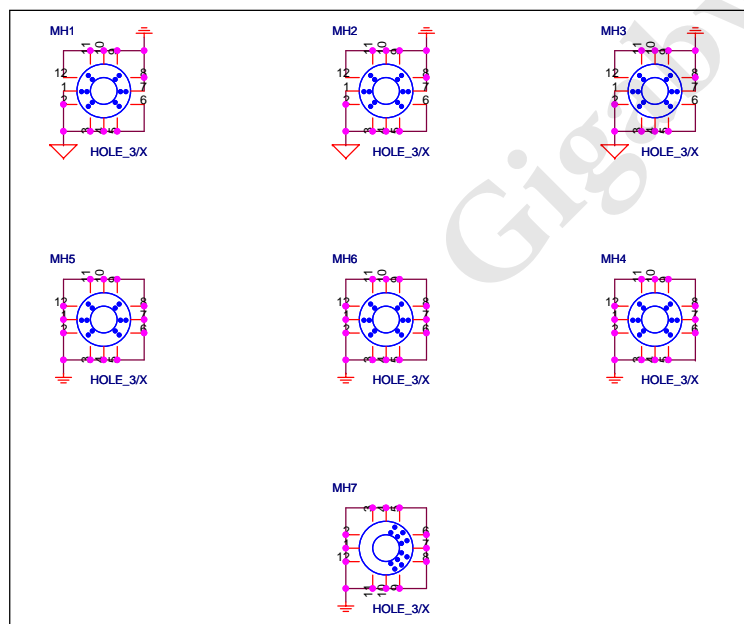
	ICH GP22	ICH GP38
NORMAL	X	X
-0.05V	L	X
-0.10V	X	L
-0.15V	L	L



ATX POWER CONNECTOR



螺絲孔位置圖 (注意Footprint不同)



Gigabyte Technology

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VCC1.8V=1.8V

VCC1.8V

VCC3

RQ1

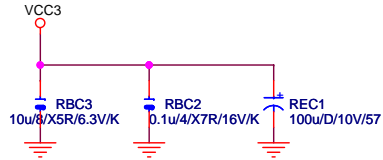
RR1 100k/4/1

RR2 44.2k/4/1

REC2 100uF/10V/5/

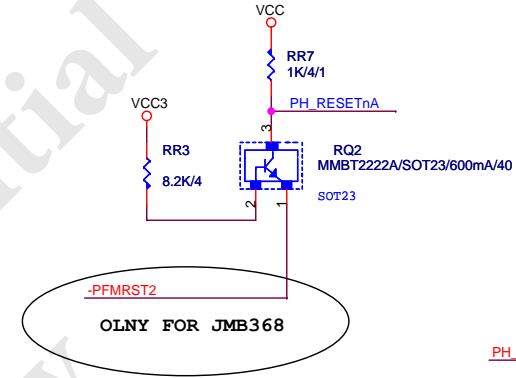
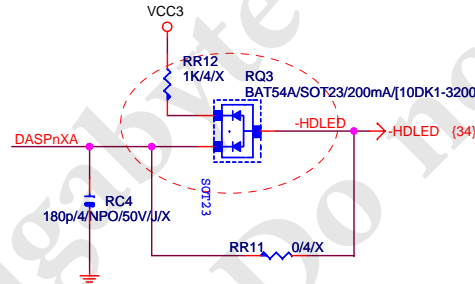
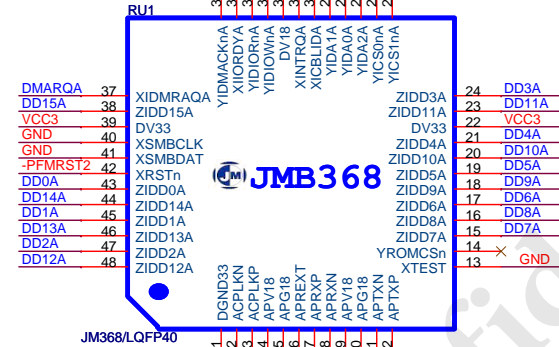
RBC1 10uF/8V/5R/6.3V/K

RBC6 0.1uF/4V/7R/16V/K



CLOSE TO pin22

close to pin17



PH_IORDY RR4 1K/4/1 VCC3

CSELA RR10 0/4/SHTX

PH_DMARQ RR6 8.2K/4

PH_INTROQ RR5 8.2K/4

DD7A RR8 8.2K/4

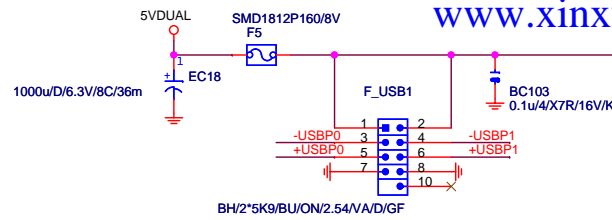
PH_IORDY	IORDYA
PH_DMARQ	DMARQA
PH_INTRQ	INTRQA
PH_CBLID_N	PDIAGnA

Pin	Signal
1	PH RESETA
2	PH DD8
3	PH DD7
4	PH DD9
5	PH DD6
6	PH DD5
7	PH DD10
8	PH DD4
9	PH DD11
10	PH DD3
11	PH DD12
12	PH DD2
13	PH DD13
14	PH DD1
15	PH DD14
16	PH DD0
17	PH DD15
18	(#20 key-pin)
19	PH DMARQ
20	PH DIOW N
21	PH DIOR N
22	(#28 CSEL)
23	PH IORDY
24	CSELA
25	PH DMACK N
26	PH INTRQ
27	PH DA1
28	(#32 IOCS16)
29	PH DA0
30	PH CS0 N
31	PH DA2
32	PH CS1 N
33	DASPhXA
34	
35	
36	
37	
38	
39	
40	

BH/2*20K20/WH/SHN/2.54/VA/PA46

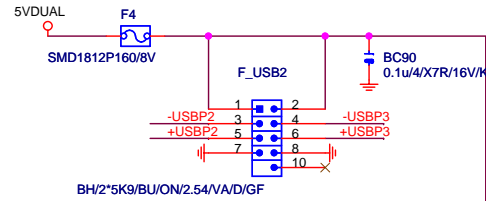
FRONT USB1

(19) +USBP0 <-> +USBP0
(19) -USBP0 <-> -USBP0
(19) +USBP1 <-> +USBP1
(19) -USBP1 <-> -USBP1

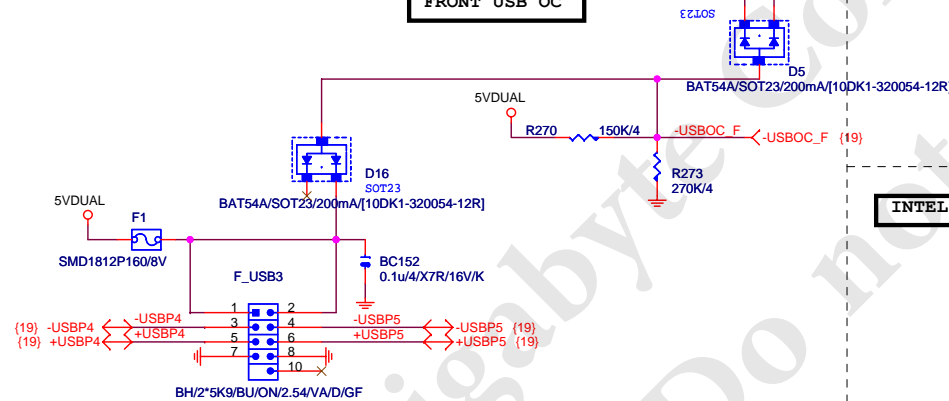


FRONT USB2

(19) +USBP2 <-> +USBP2
(19) -USBP2 <-> -USBP2
(19) +USBP3 <-> +USBP3
(19) -USBP3 <-> -USBP3

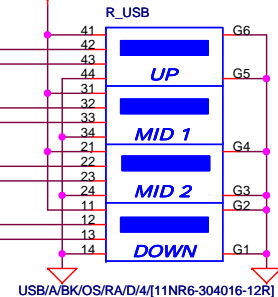


FRONT USB3

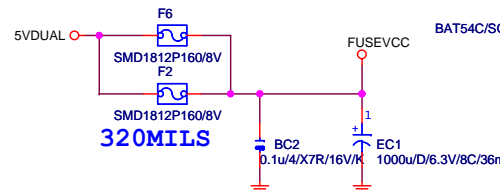


REAR USB

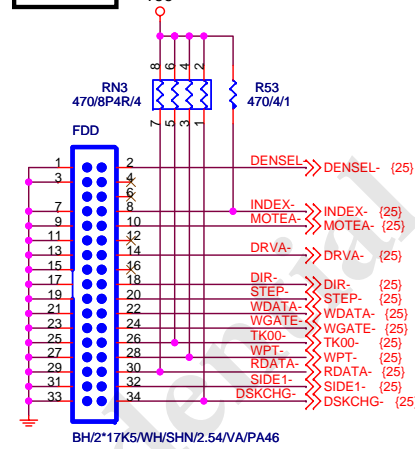
(19) -USBP8 <-> -USBP8
(19) +USBP8 <-> +USBP8
(19) -USBP9 <-> -USBP9
(19) +USBP9 <-> +USBP9
(19) -USBP10 <-> -USBP10
(19) +USBP10 <-> +USBP10
(19) -USBP11 <-> -USBP11
(19) +USBP11 <-> +USBP11



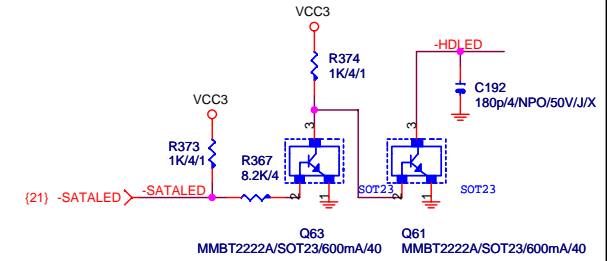
USB POWER



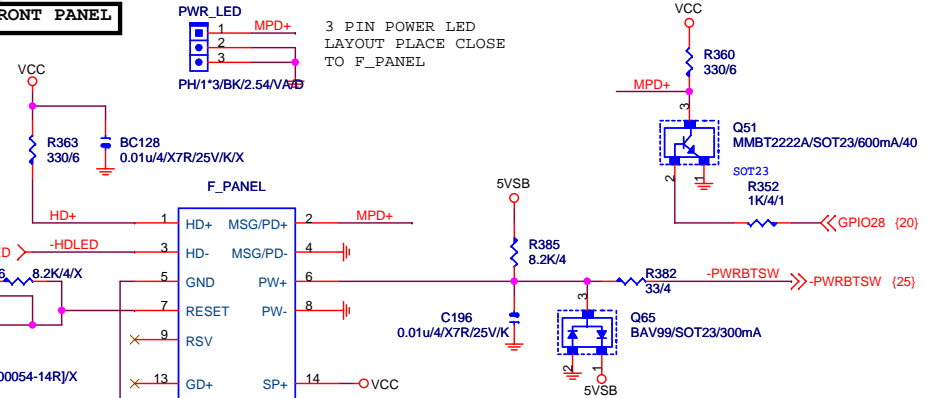
FLOPPY



SATA LED



INTEL FRONT PANEL



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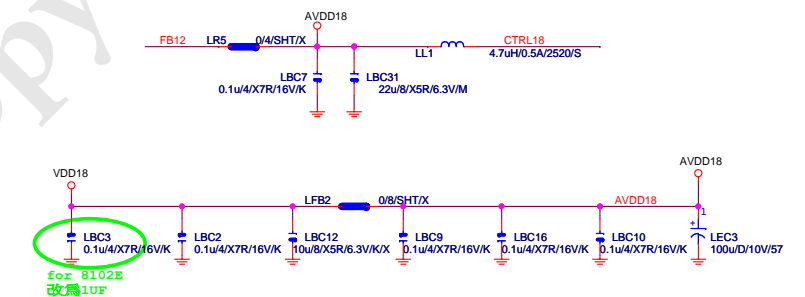
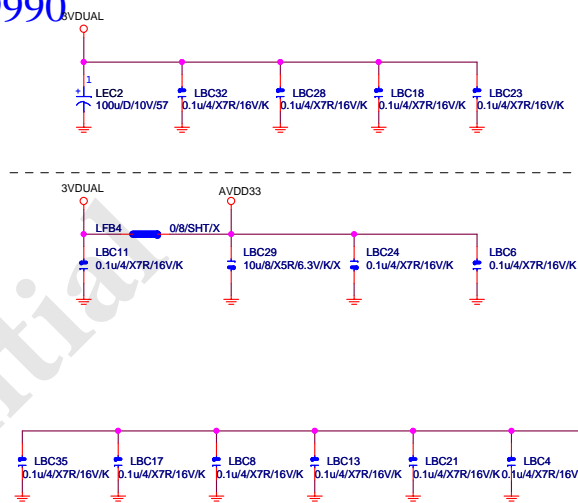
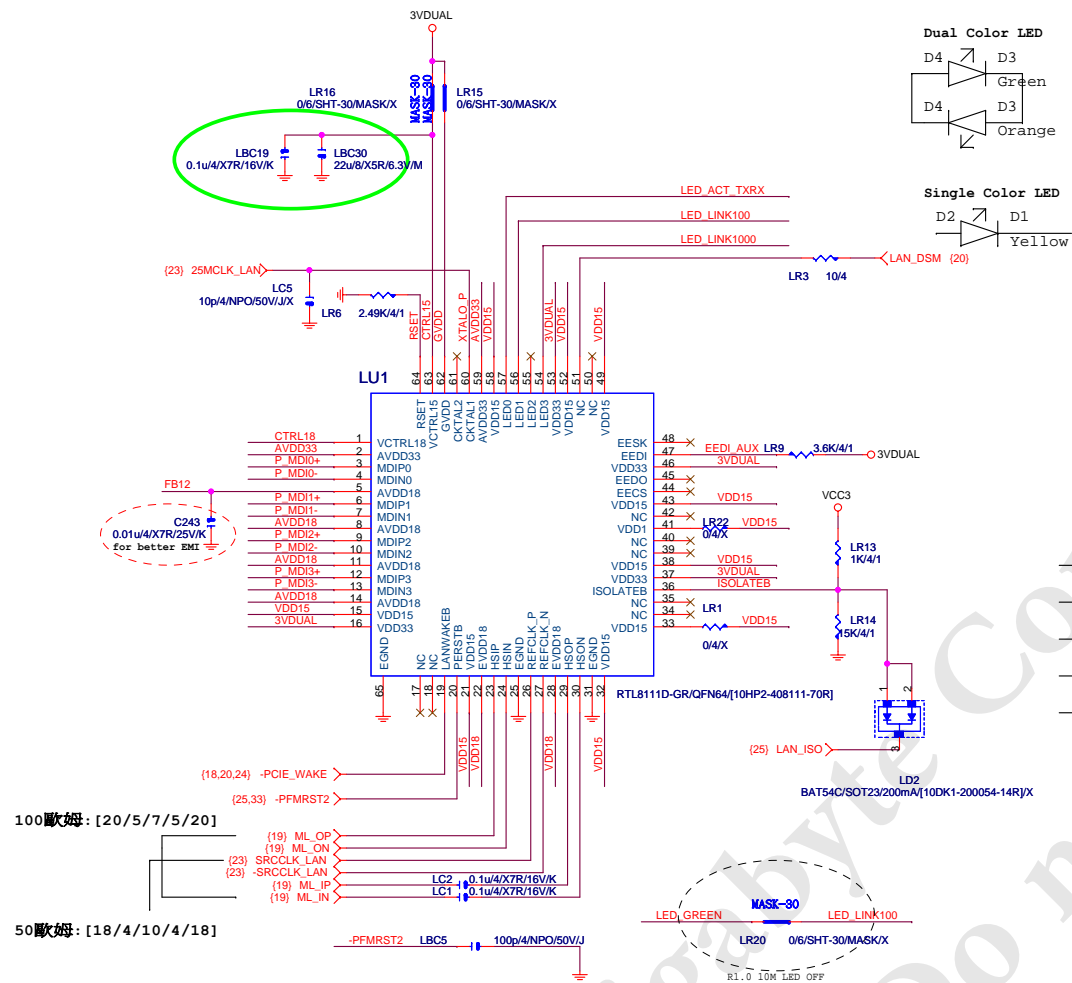
FP,USB,USB PWR,FDD,BZ

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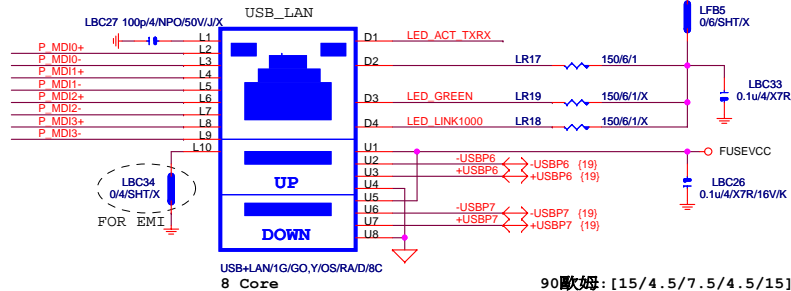
Rev 1.0

PCIE-1G LAN



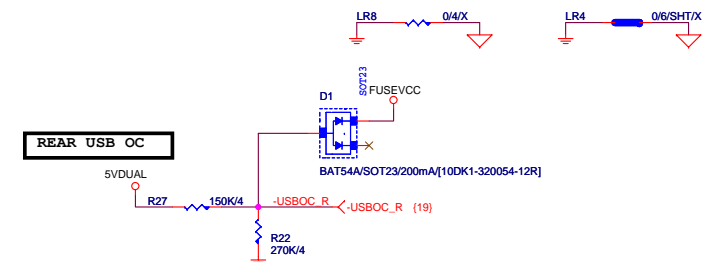
USB LAN CONNECTOR

LAN 100欧姆: [30/4/8/4/30] FOR B 製程



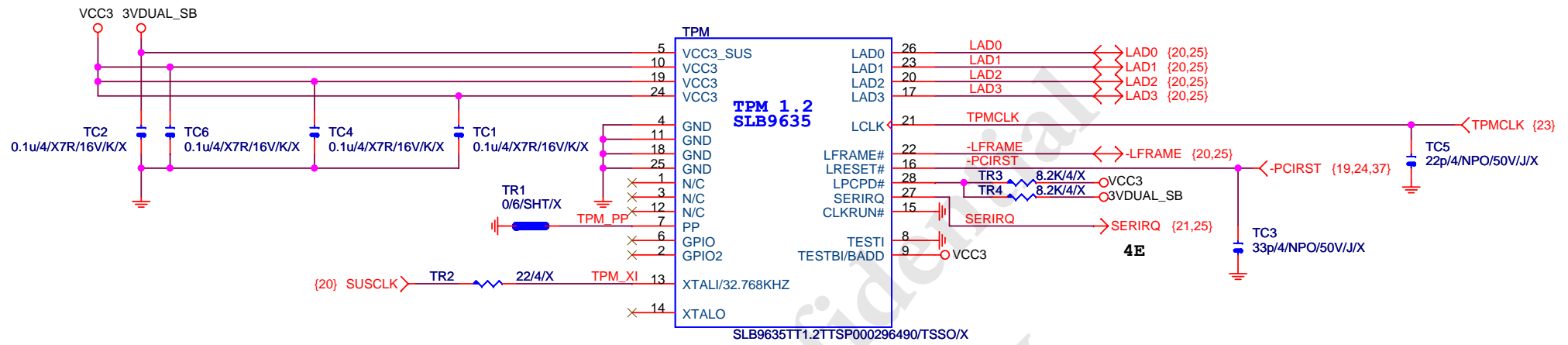
USB POWER

REAR USB OC



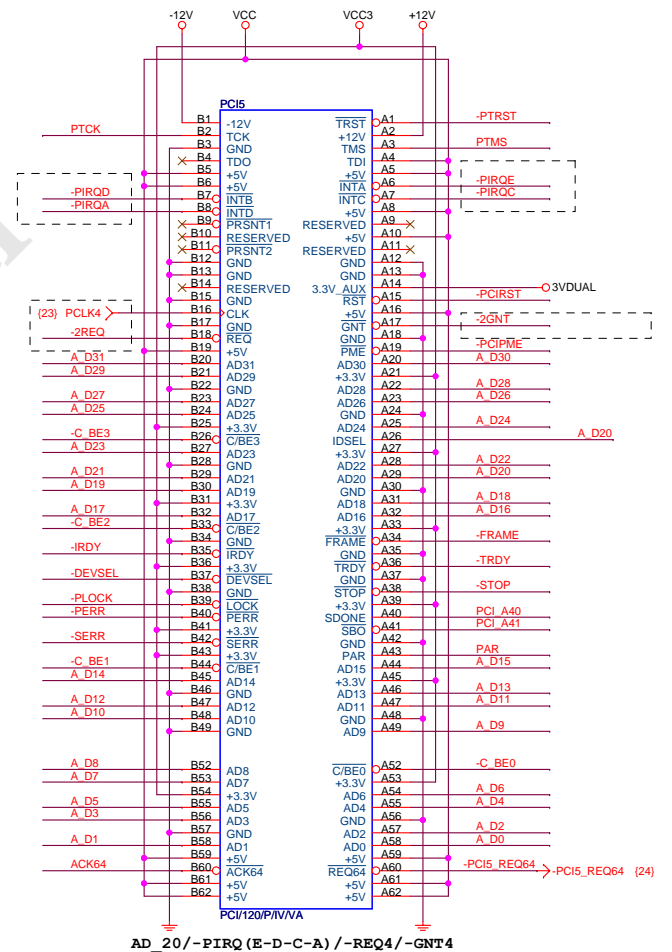
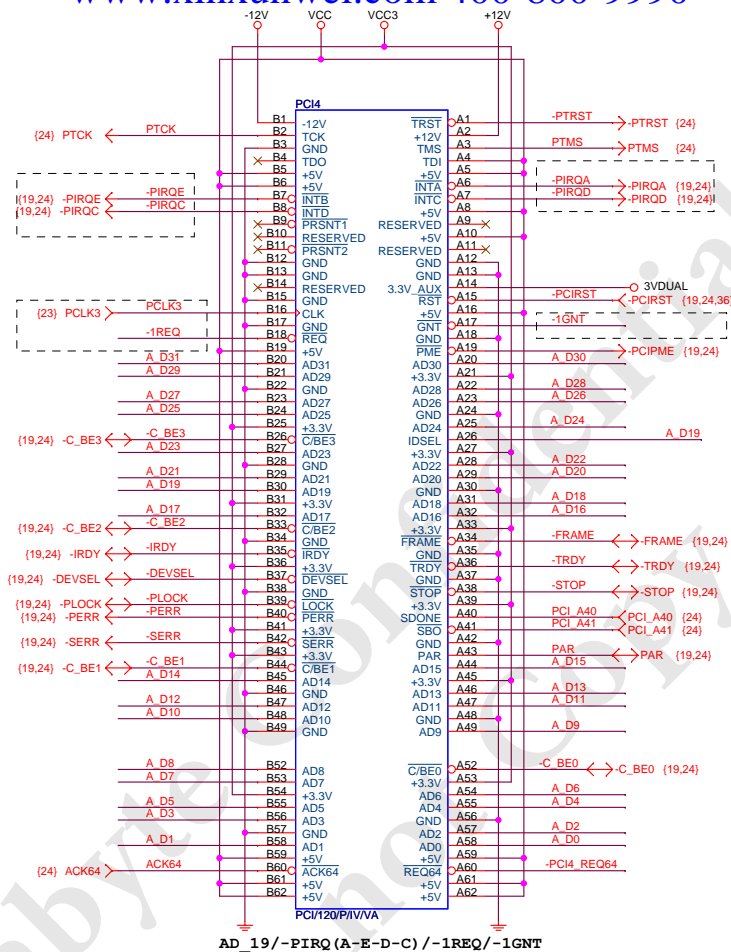
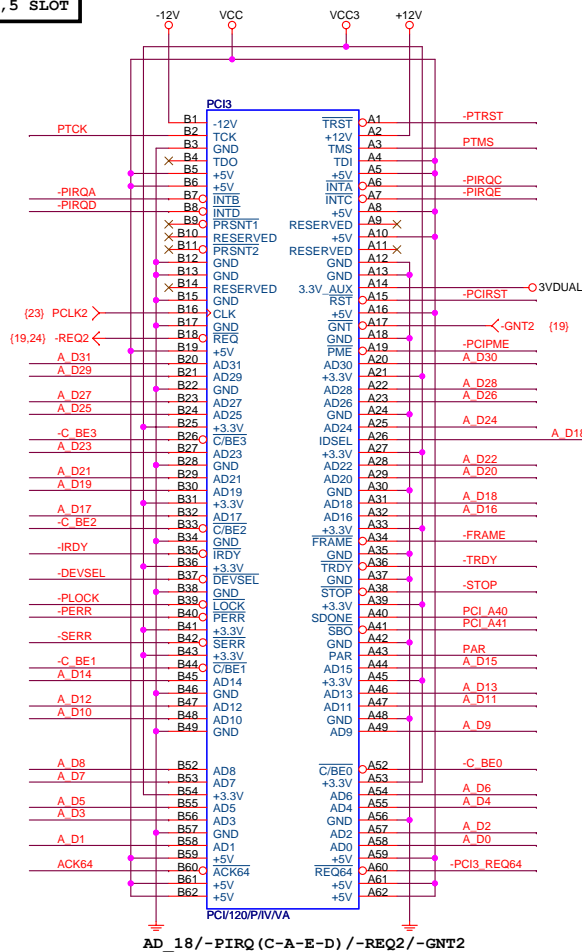
Gigabyte Technology

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Size			Custom
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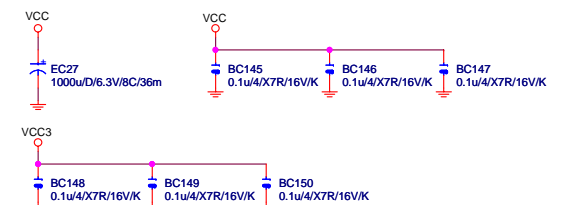
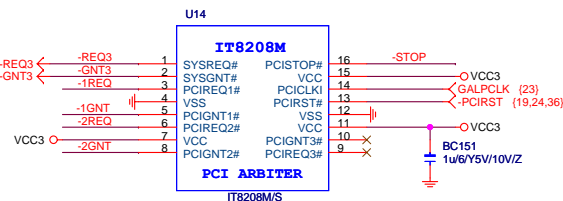
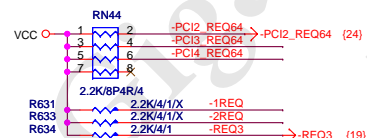
**GIGABYTE THCHNOLOGIES**

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TPM I/F-SLB 9635 TT 1.2		
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PCI 3,4,5 SLOT



(19,24) A_D[0..31] ↔ A_D[0..31]



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PCI SLOT 3, 4, 5		
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